PFL-A-02
phyFLEX-i.MX 6

PHYTEC

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

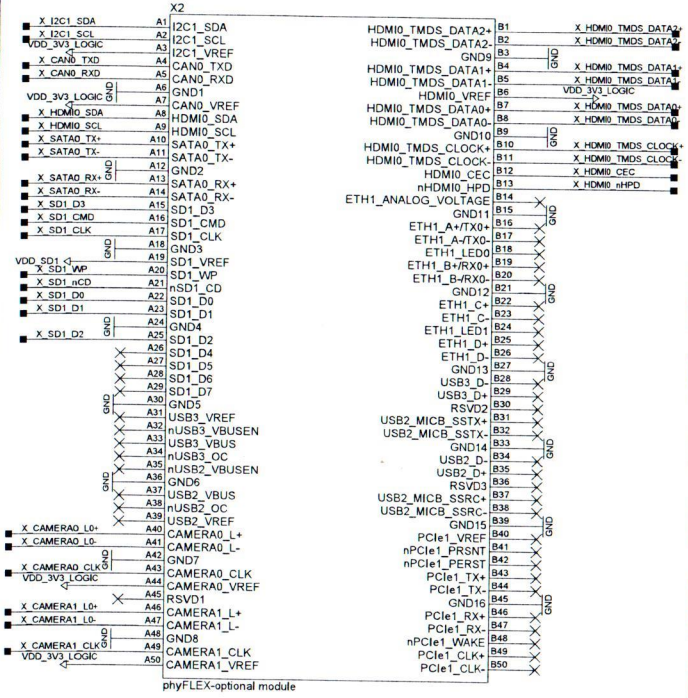
Project: PFL-A-02 phyFLEX-i.MX 6

Department: F&E
Author: M.Dzierzawa

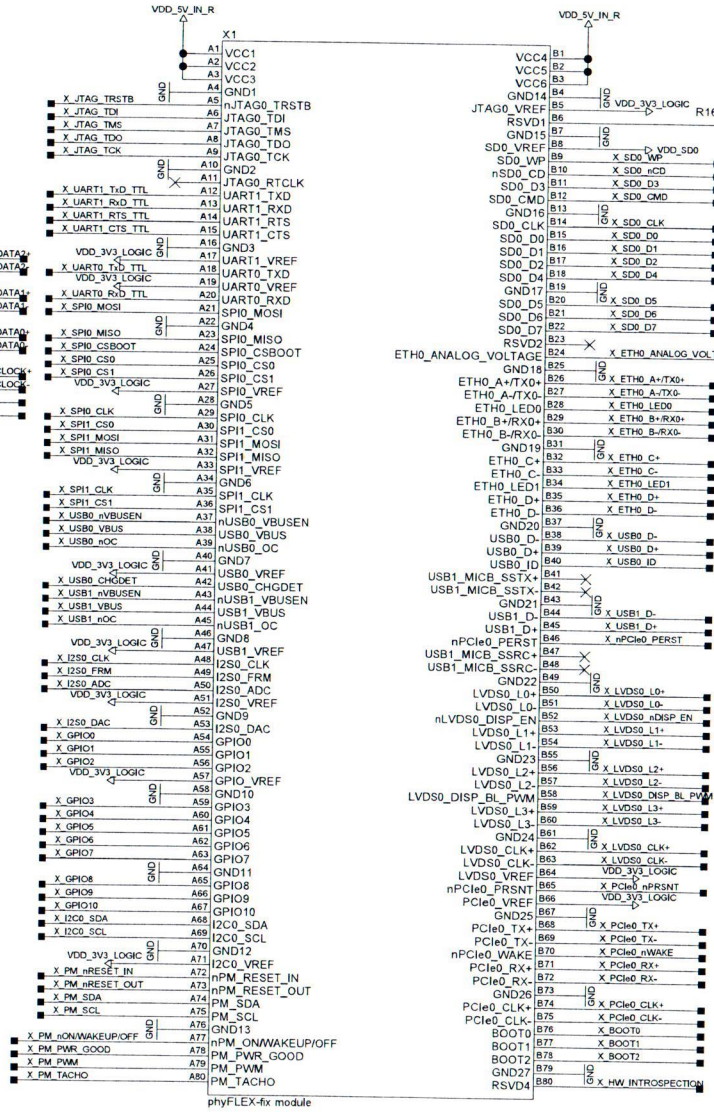
01.10.2013 | PCB-No.: 1362.2 | Revision: 002 | Sheet 1 of 18

Connector

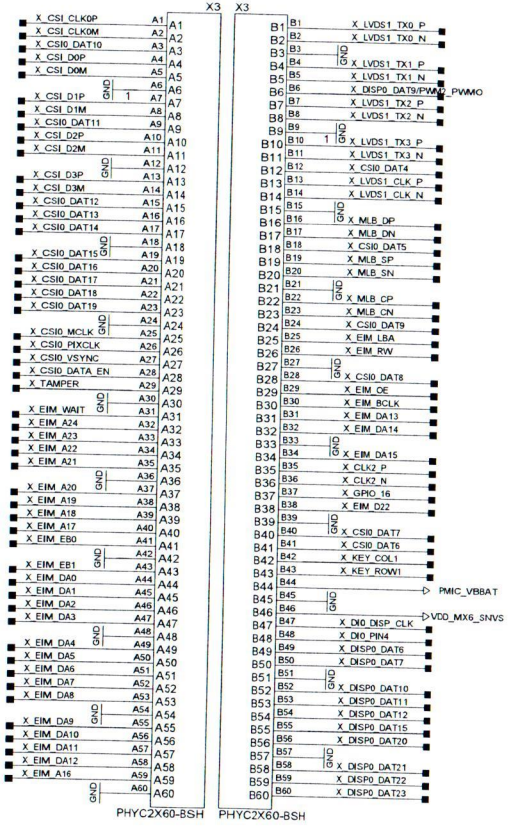
phyFLEX-optional

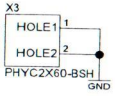


phyFLEX-fix

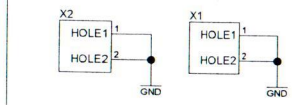


phyFLEX-flex



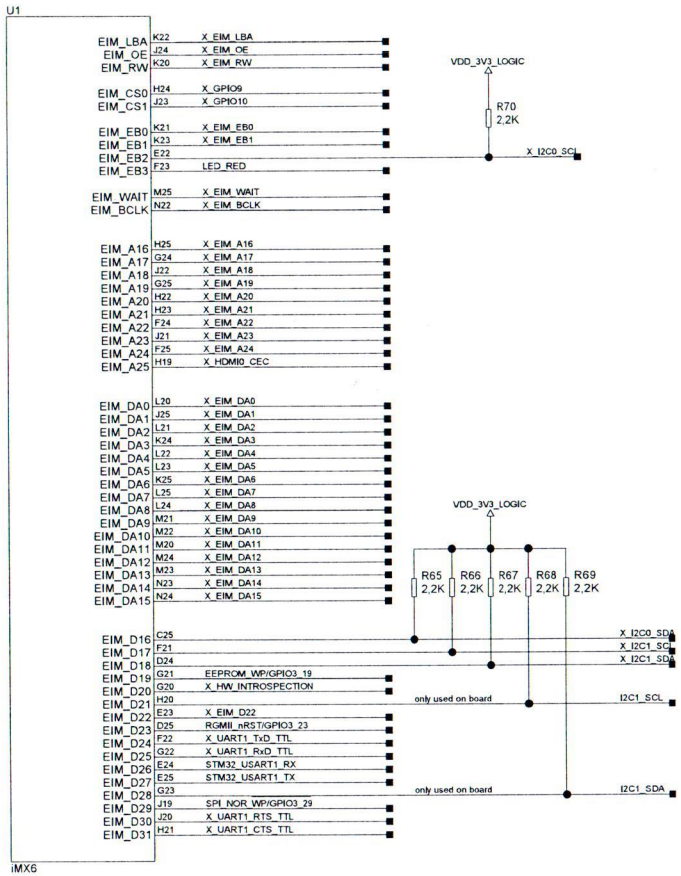


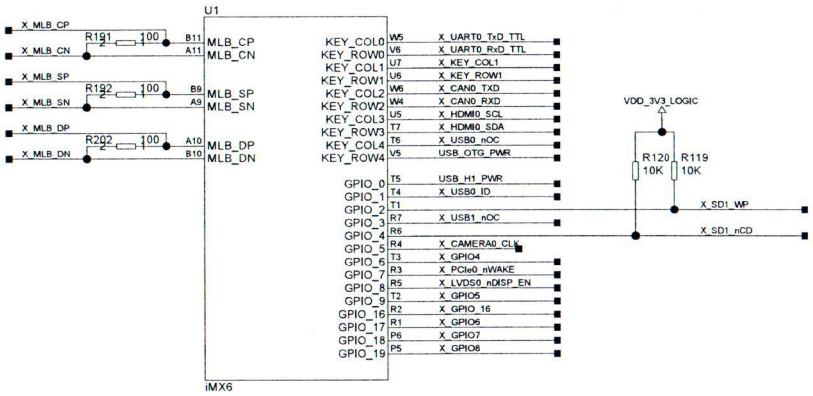
Holes for X1 and X2 are the same!

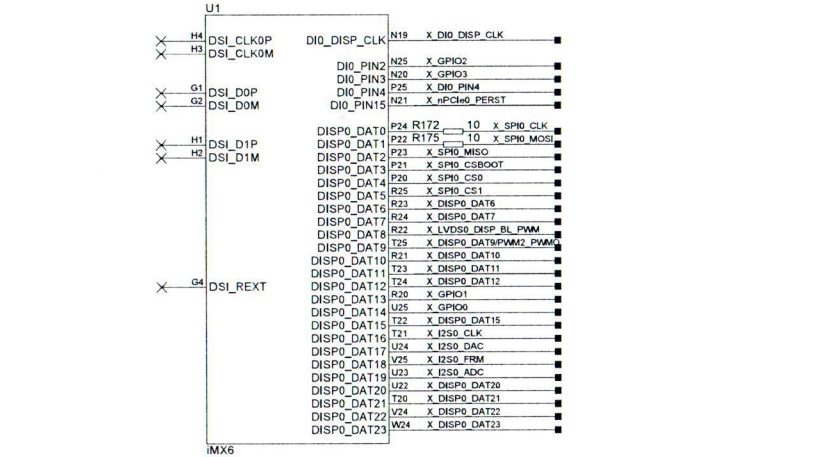


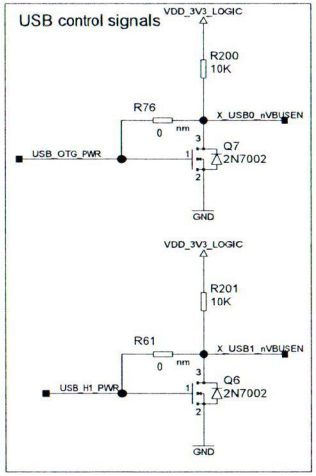
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz
Project: PFL-A-02 phyFLEX-i.MX 6		Department : F&E Author: M.Dzierzawa
01.10.2013	PCB-No.: 1362.2	Revision :002 Sheet 2 of 18

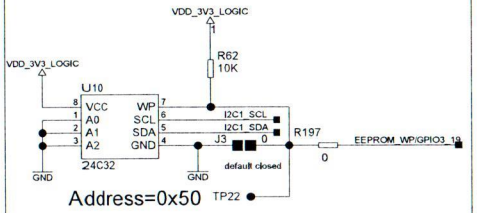
SPI, I2C, UART, CAN, I2S, EEPROM, SPI-Flash

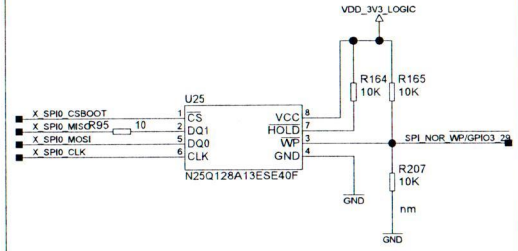


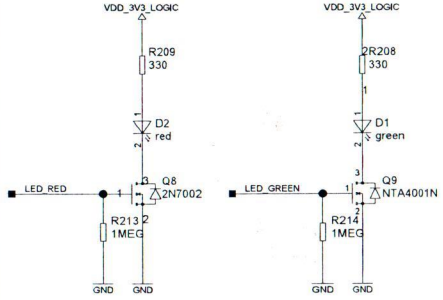










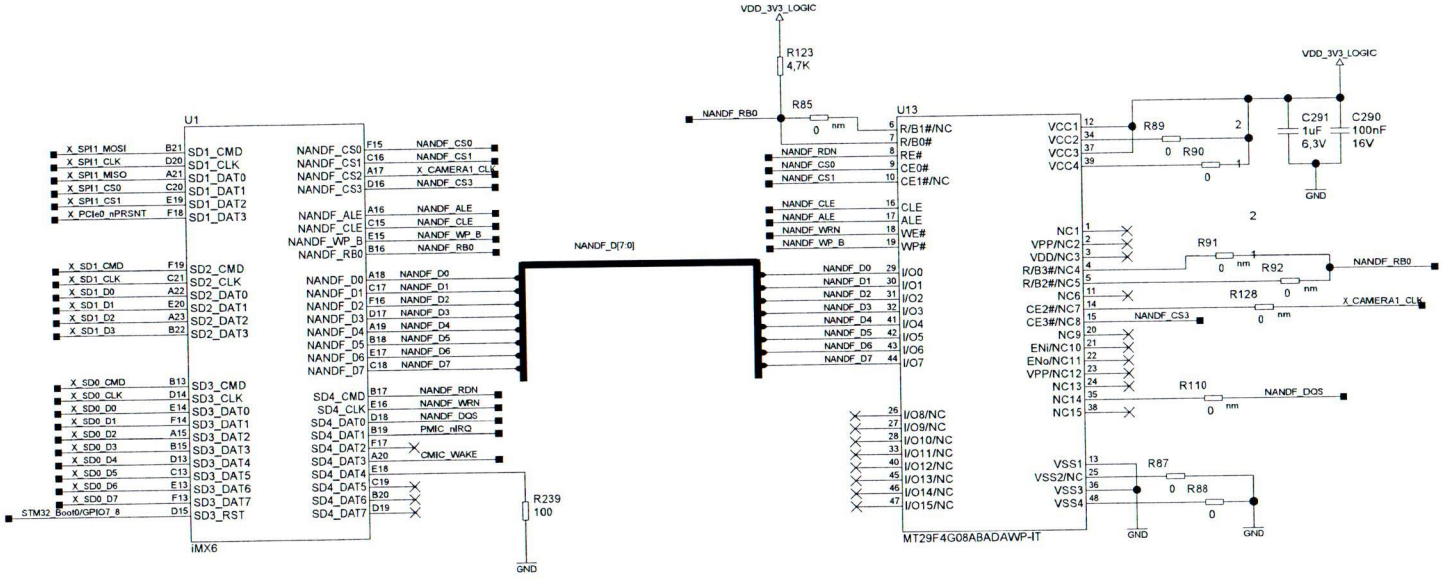


PHYTEC

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

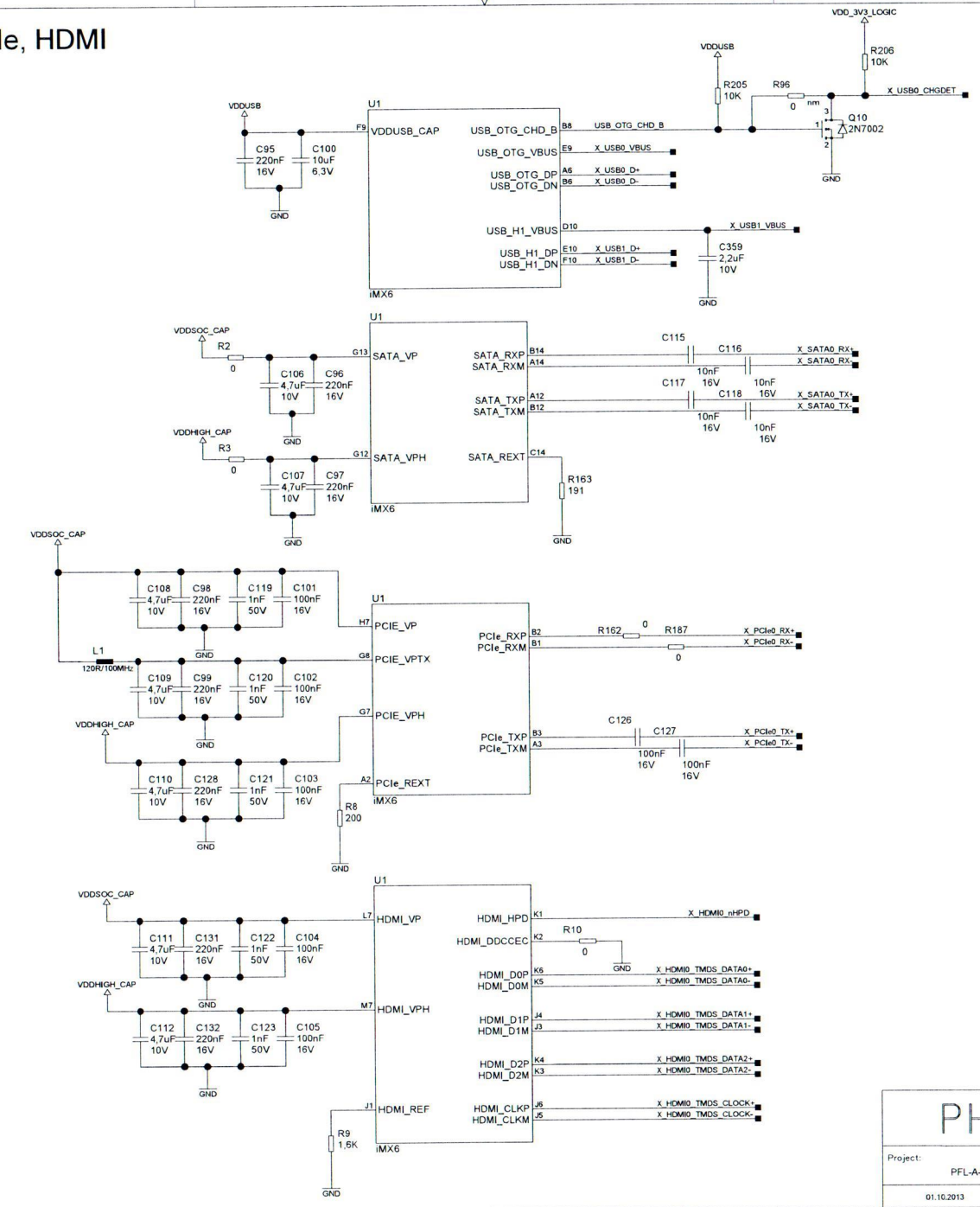
Project: PFL-A-02 phyFLEX-i.MX 6		Department : F&E	
		Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision 002	Sheet 3 of 18

SDIO, NAND-Flash



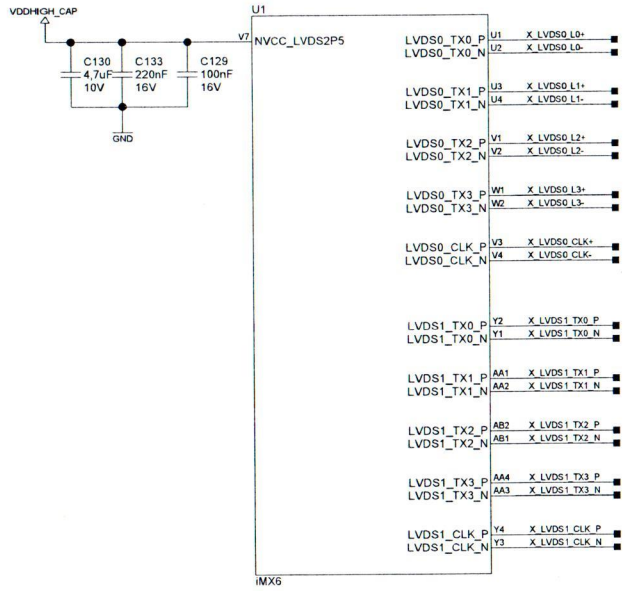
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002	Sheet 4 of 18

USB Host + OTG, SATA, PCIe, HDMI

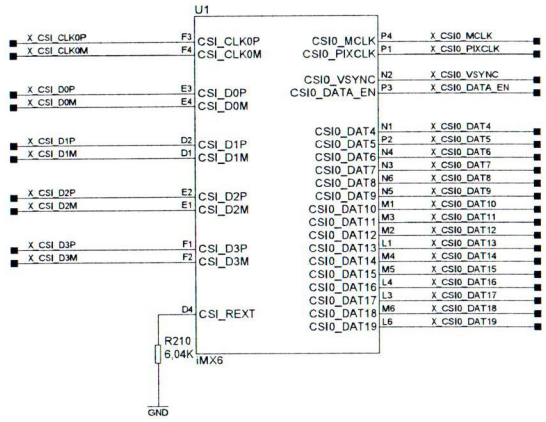


PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002	Sheet 5 of 18

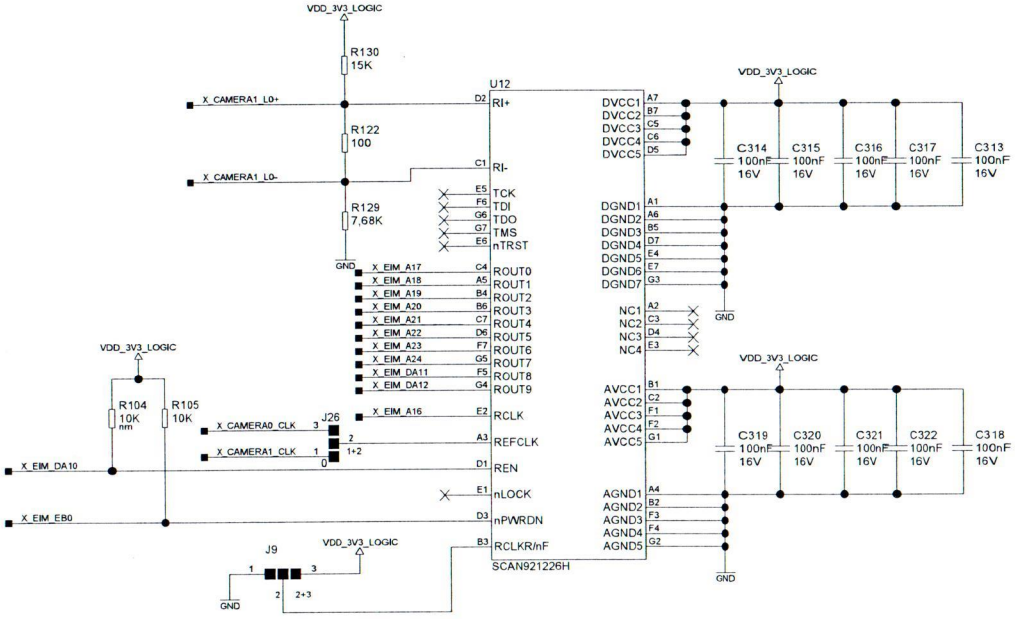
Display LVDS, Camera_0-2



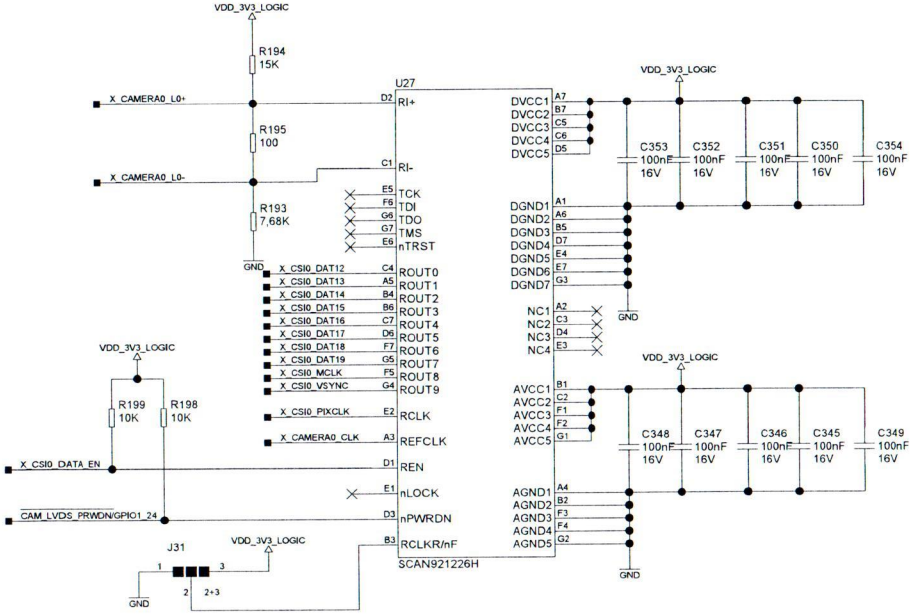
Camera_2, CSI-2 (MIPI)



Camera_1, CSI1 (parallel) <- phyCAM-S+ (LVDS)



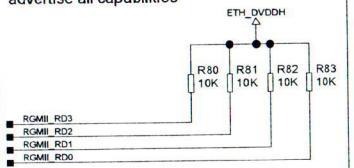
Camera_0, CSI0 (parallel) <- phyCAM-S+ (LVDS)



PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002	Sheet 6 of 18

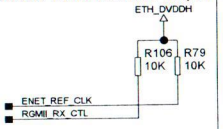
10/100/1000 Ethernet

advertise all capabilities

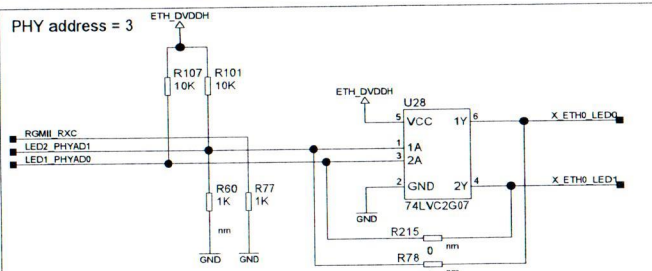


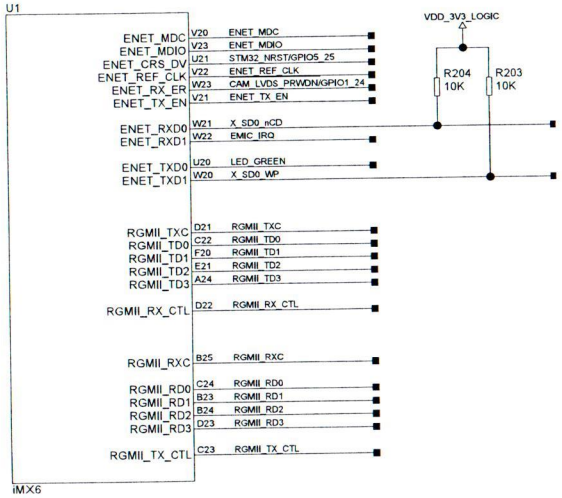
Single LED Mode

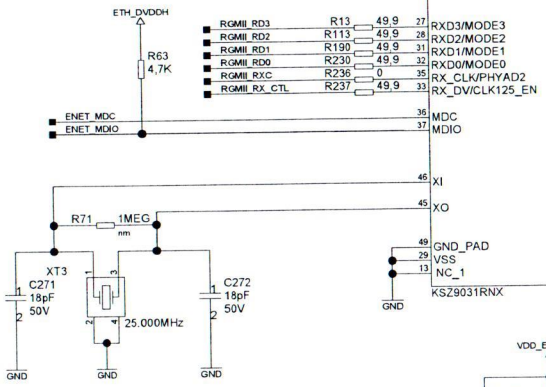
Enable 125MHz Clock output

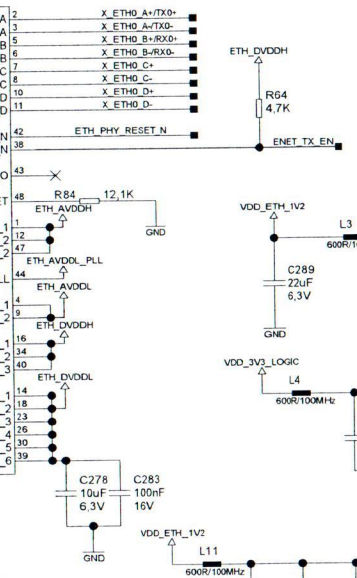


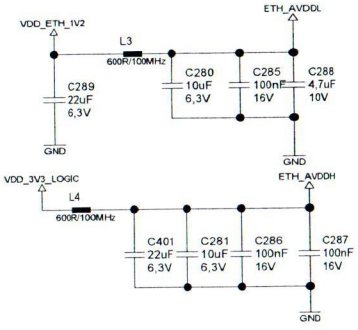
PHY address = 3

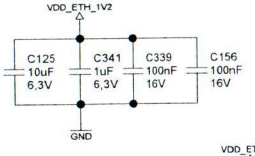


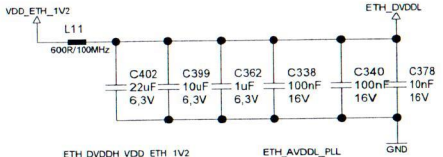


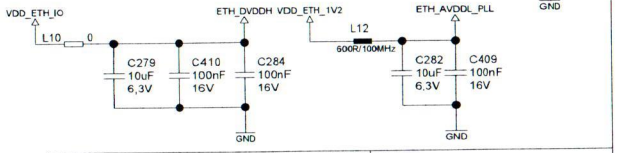


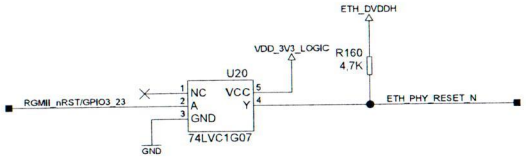






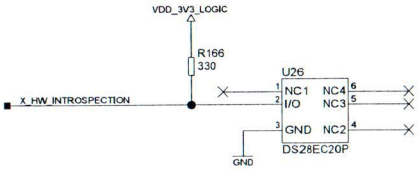


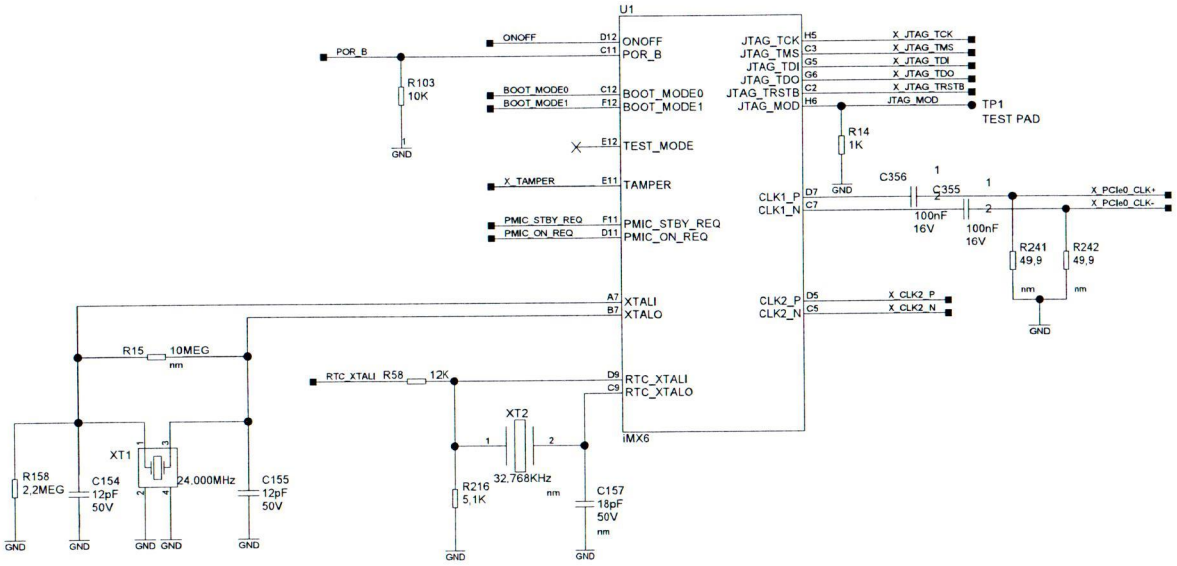


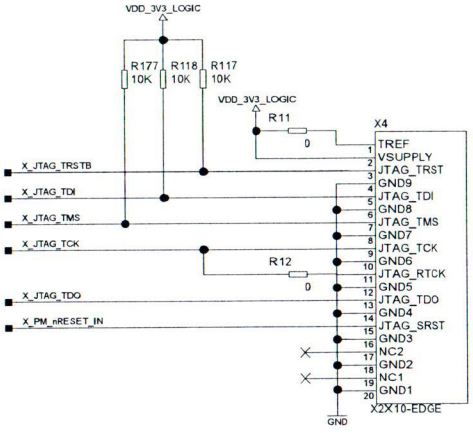


PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002	Sheet 7 of 18

i.MX6 Control

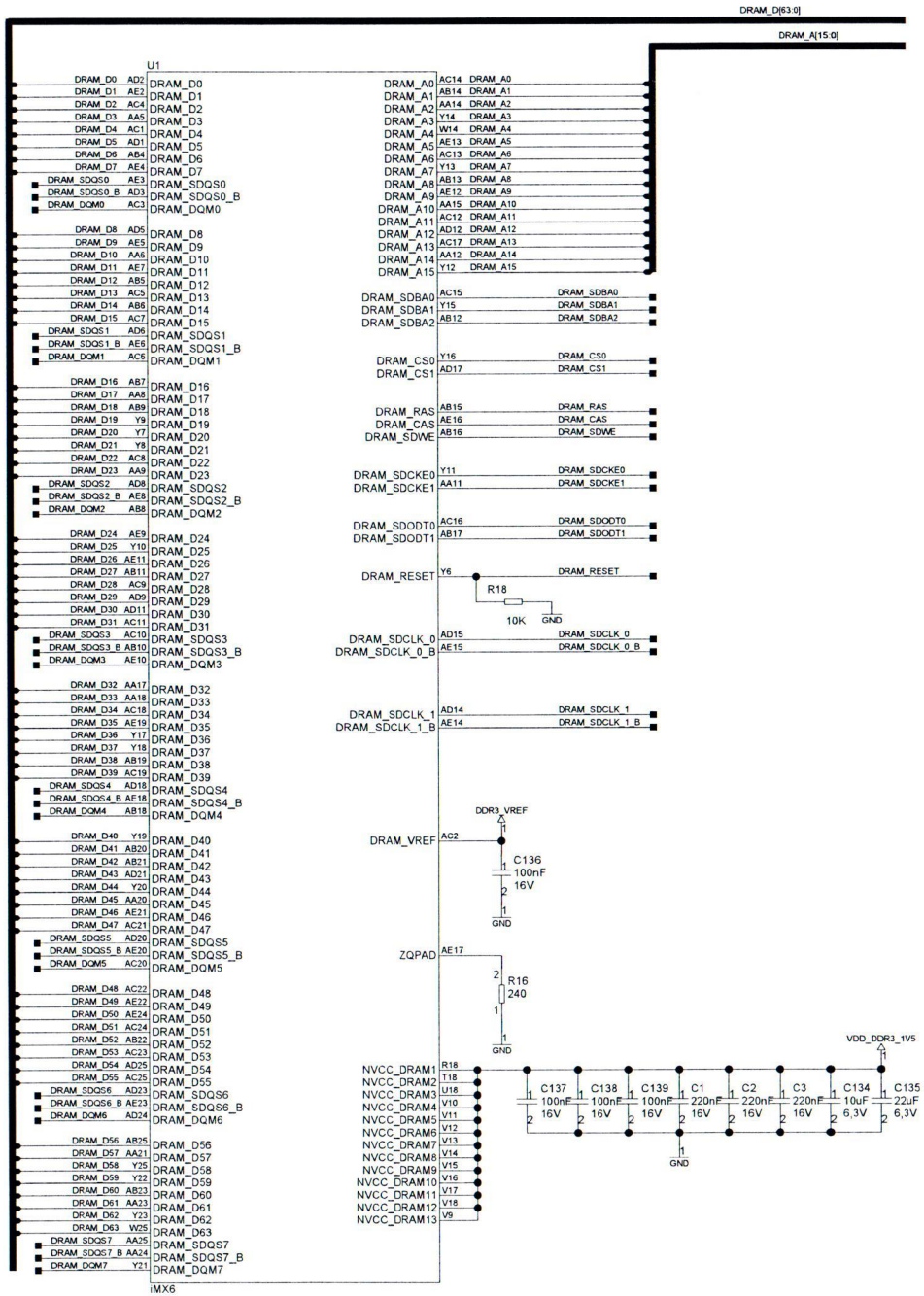




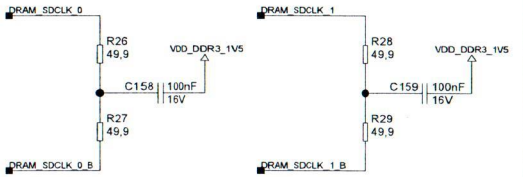


PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department : F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision : 002	Sheet 8 of 18

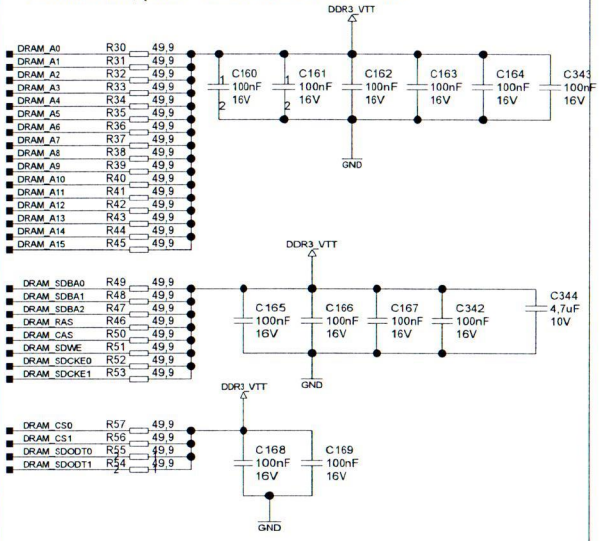
DDR3



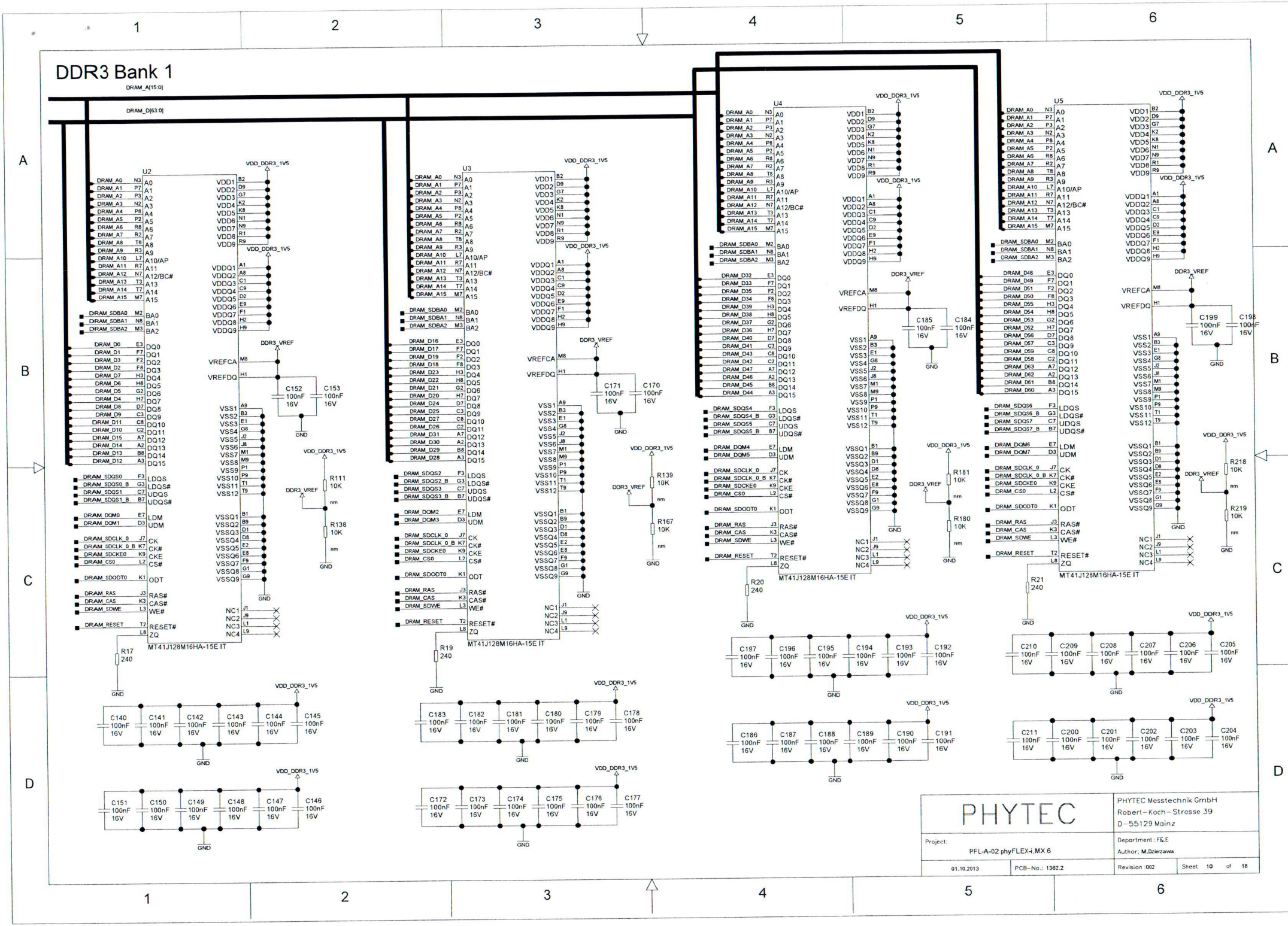
Place at the end of the route



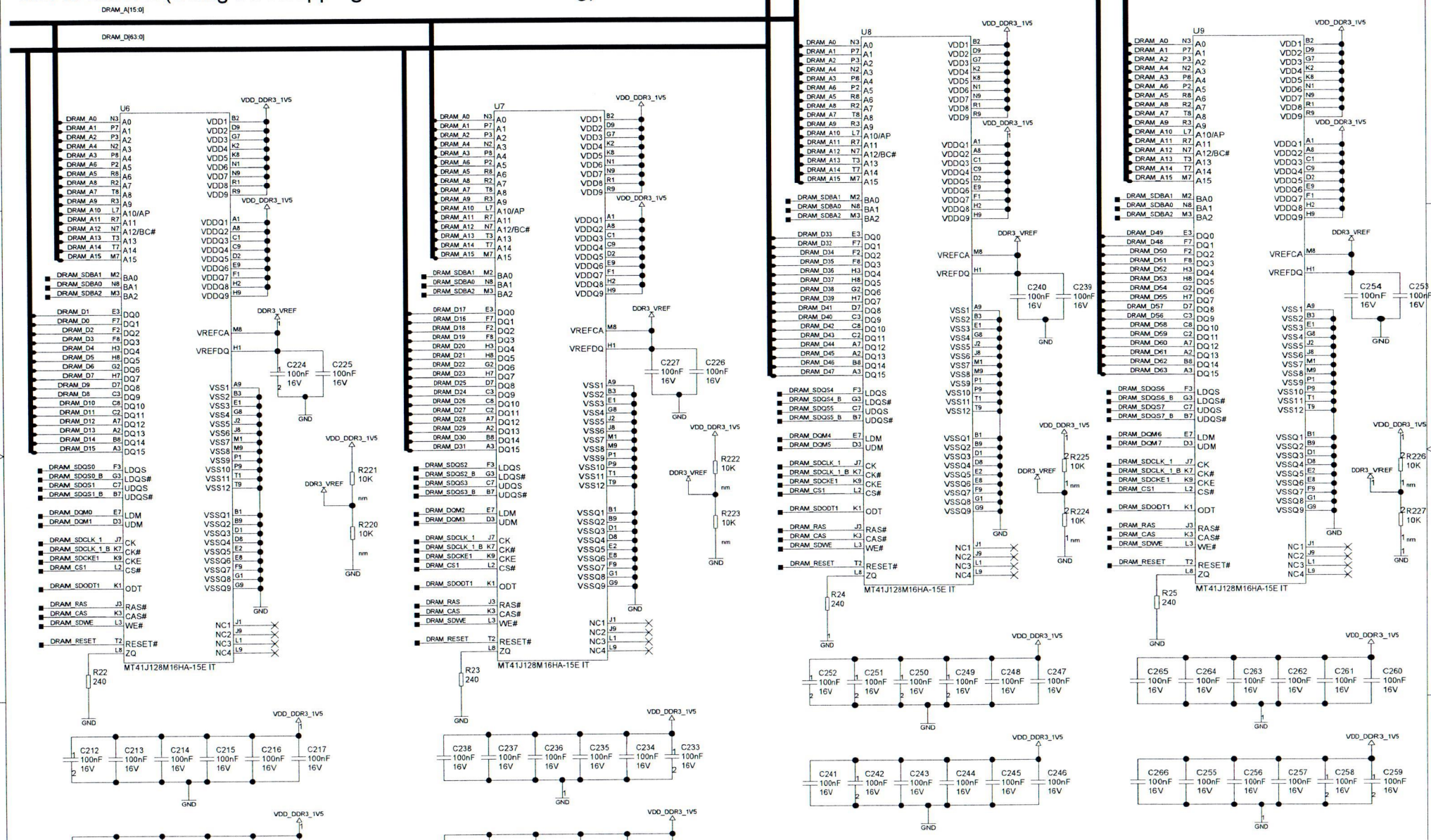
Termination, place at the end of the route



PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002	Sheet 9 of 18

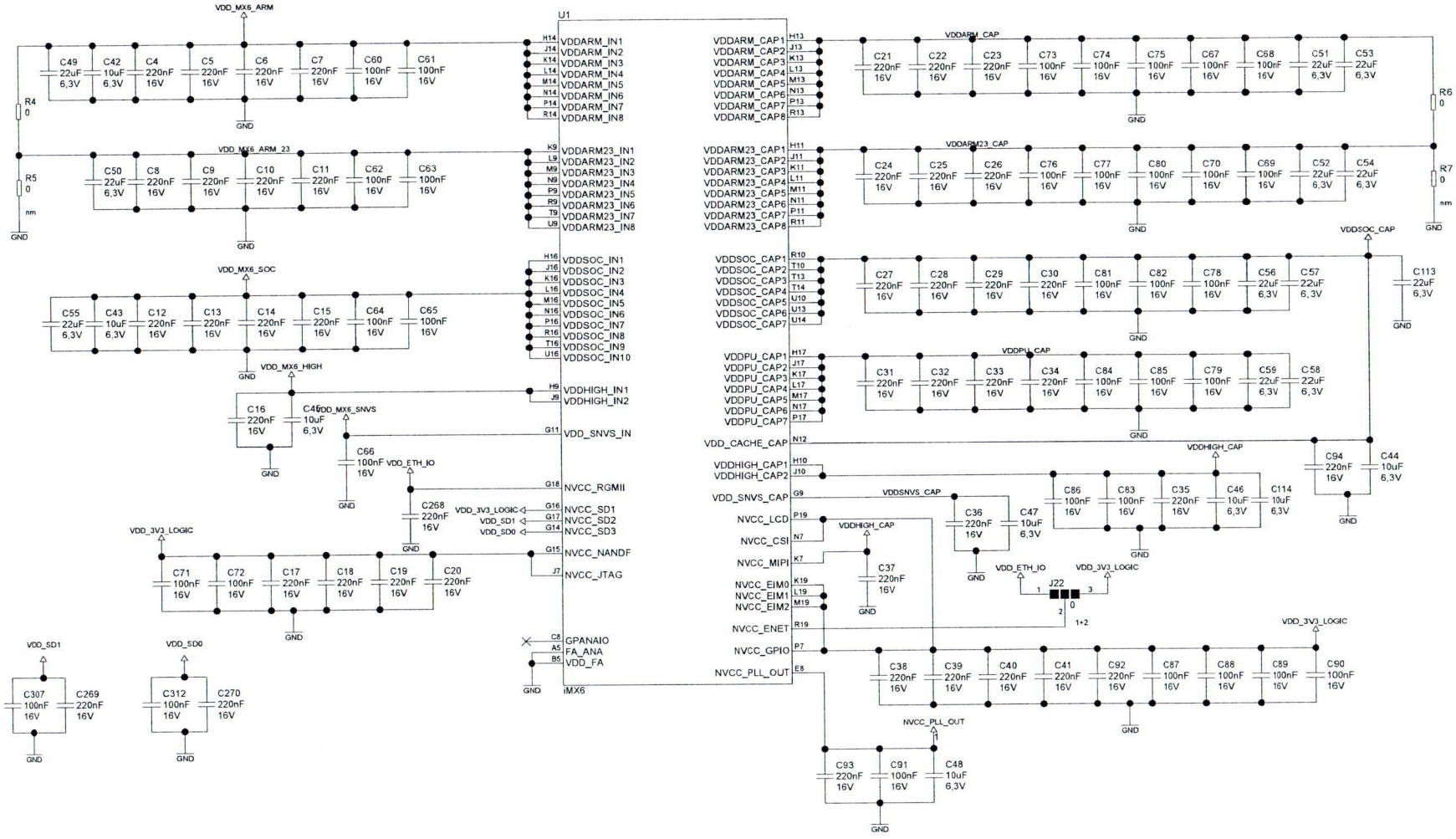

DDR3 Bank 1
DRAM_A[15:0]
DRAM_D[63:0]
U2
U3
U4
U5
MT41J128M16HA-15E IT
VDD_DDR3_1V5
DDR3_VREF
GND
PHYTEC
PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz
Project:
PFL-A-02 phyFLEX-i.MX 6
Department : F&E
Author: M.Dzierzawa
01.10.2013
PCB-No.: 1362.2
Revision :002
Sheet 10 of 18

DDR3 Bank 2 (Using bit swapping and address mirroring)



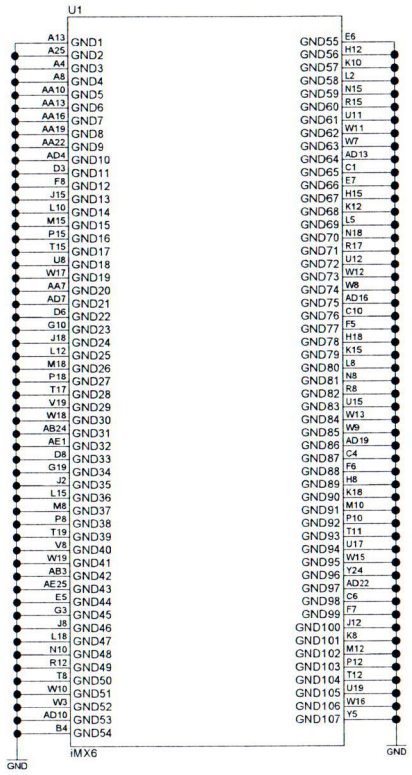
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision 002	Sheet 11 of 18

i.MX6 Power



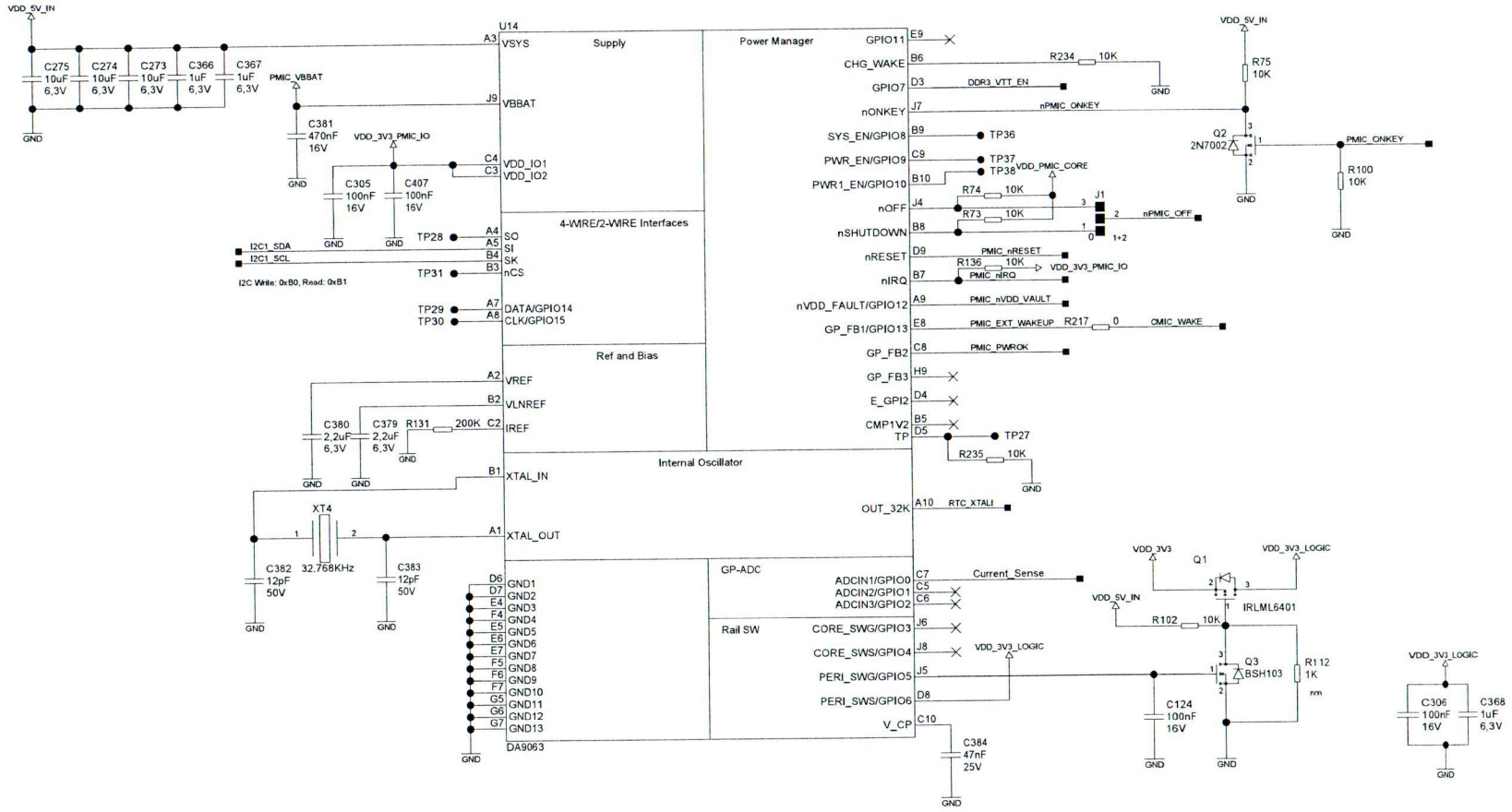
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department : F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision :002	Sheet 12 of 18

i.MX6 GND



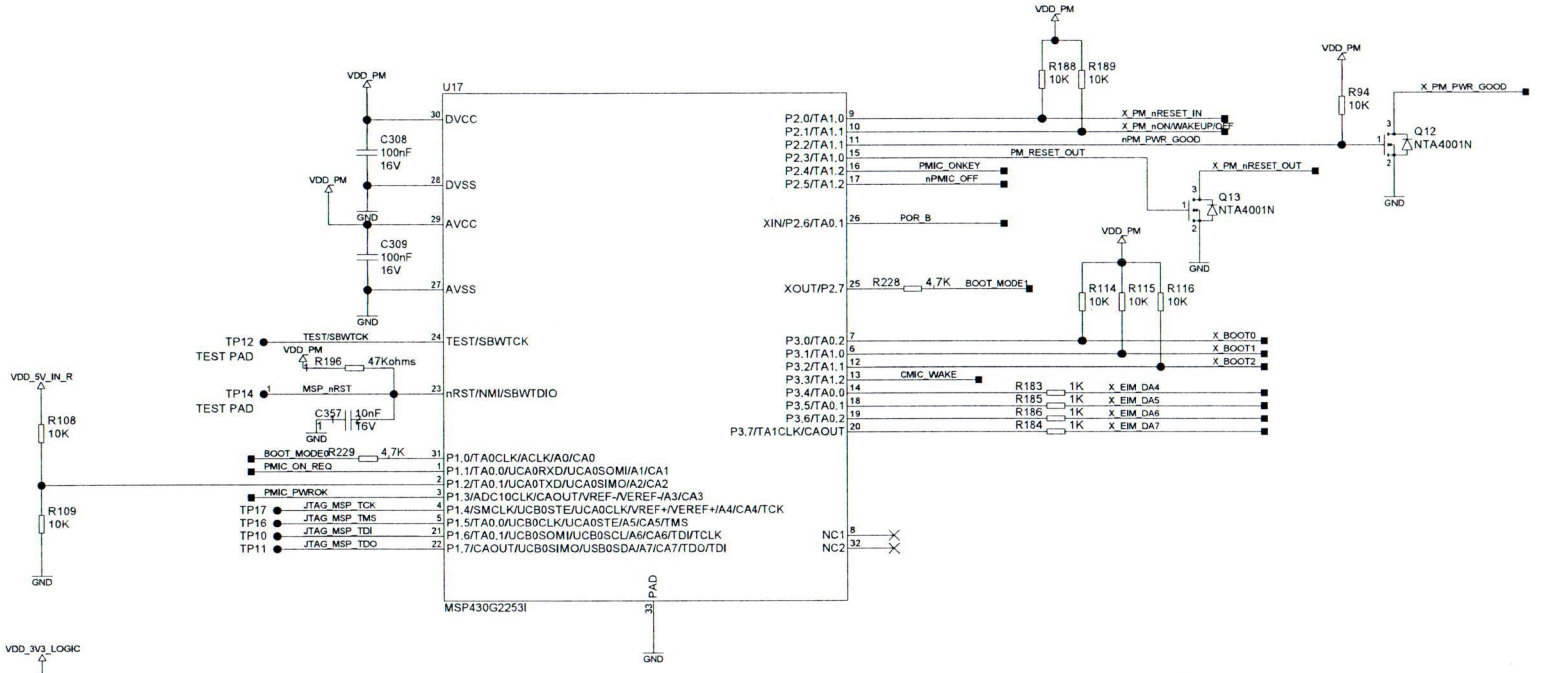
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002	Sheet 13 of 18

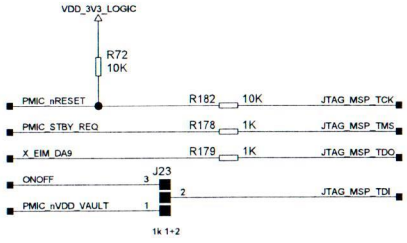
PMIC Control



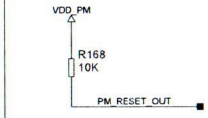
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision .002	Sheet 15 of 18

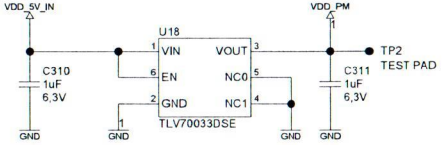
CMIC





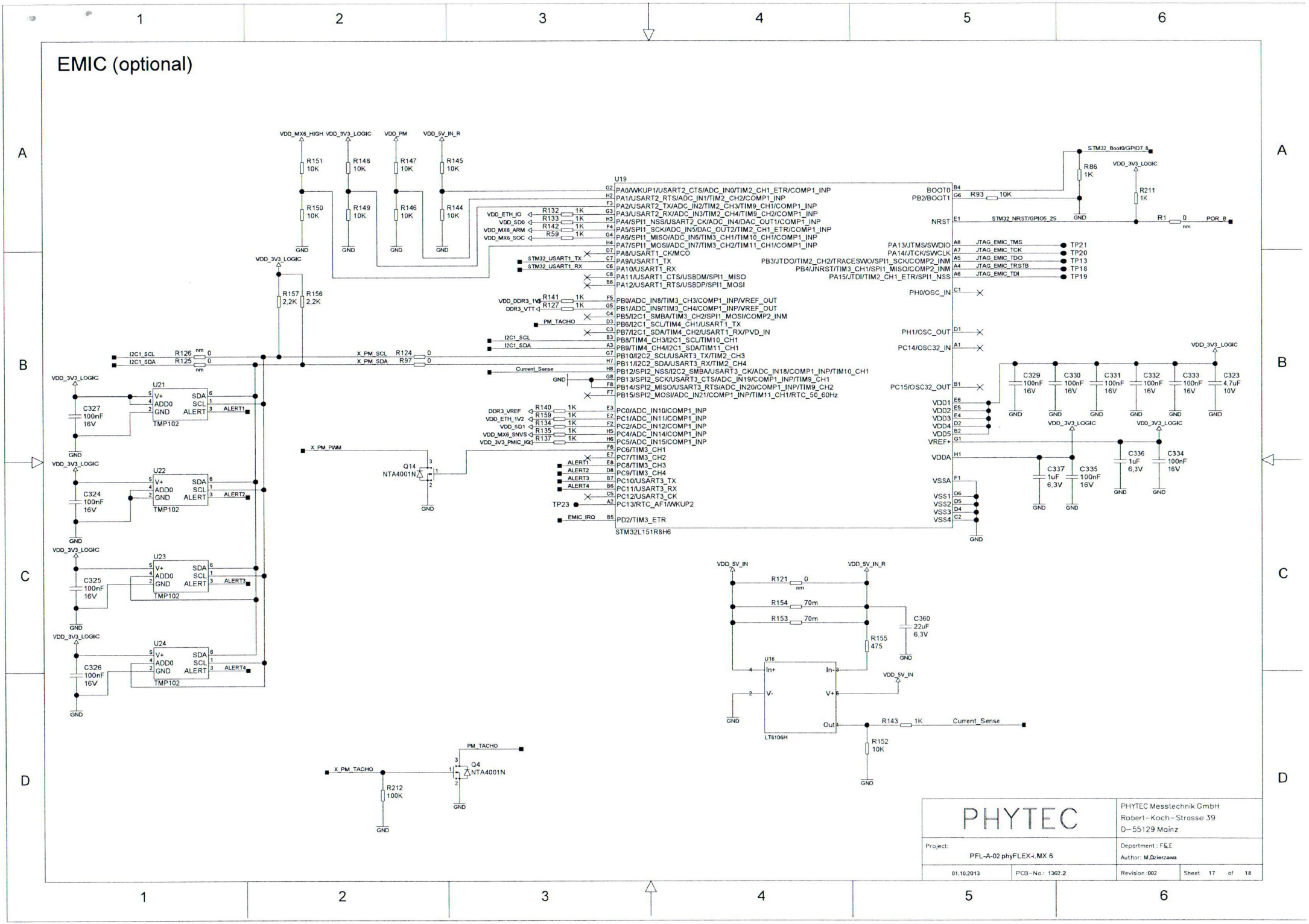
NAND Configuration Resistor:
Populated: Config 2[1]=1 (64 pages per block)
Not populated: Config 2[1]=0 (128 pages per block)
MSP activetes always internal PU





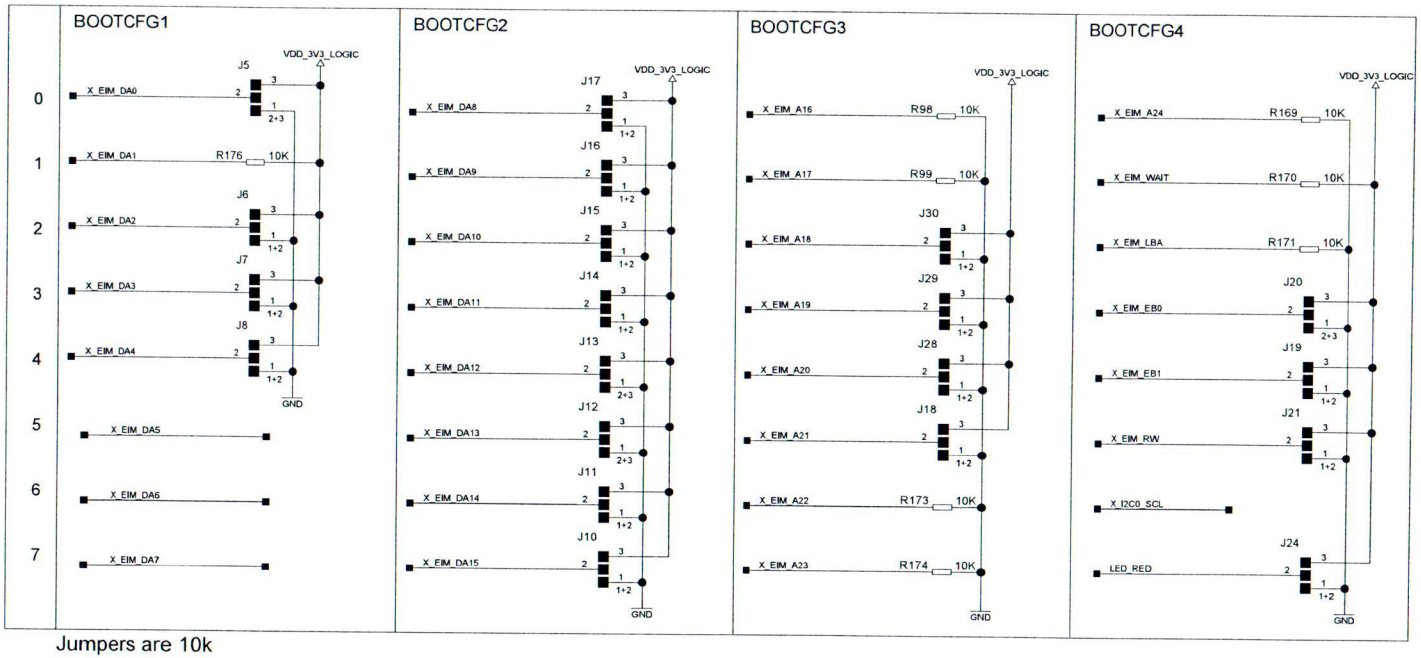
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz
Project: PFL-A-02 phyFLEX-i.MX 6		Department : F&E Author: M.Dzierzawa
01.10.2013	PCB-No.: 1362.2	Revision: 002
Sheet 16 of 18		

EMIC (optional)



PHYTEC	PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6	Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision :002 Sheet 17 of 18

Boot Configuration



Jumpers are 10k

default:

	config1[7:0]	config2[7:0]	config3[7:0]	config4[7:0]
NAND 4/8Gb (64 pages per block):	????0011	00110010	00000000	01001010

(? means that this bit is set by the MSP according to the X_BOOT pins)

NAND configuration:

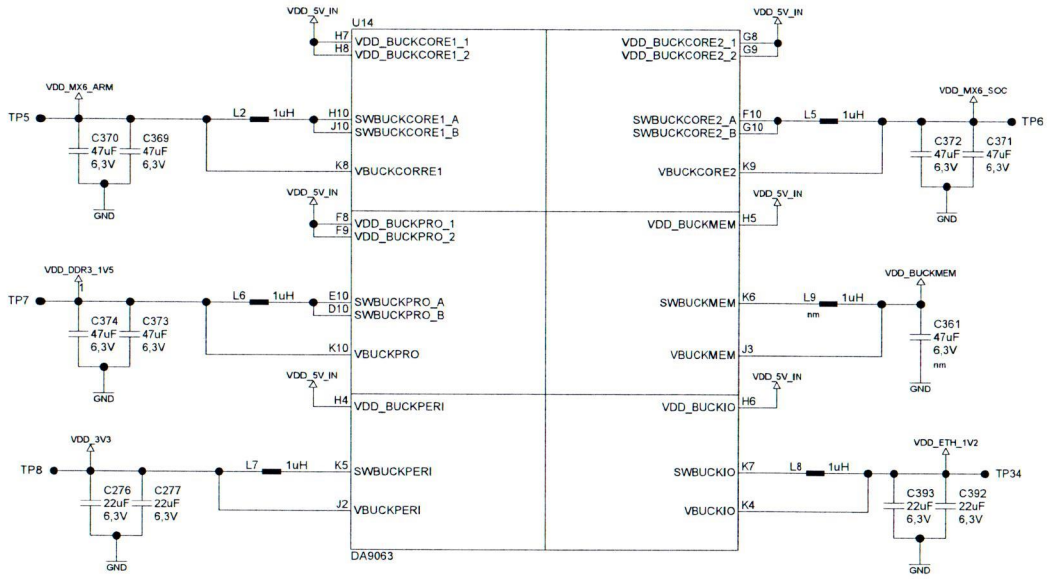
	config1[7:0]	config2[7:0]	config3[7:0]	config4[7:0]
NAND 4/8Gb (64 pages per block):	10000011	00110010	00000000	01001010
NAND 16/32Gb (128 pages per block):	10000011	00110000	00000000	01001010

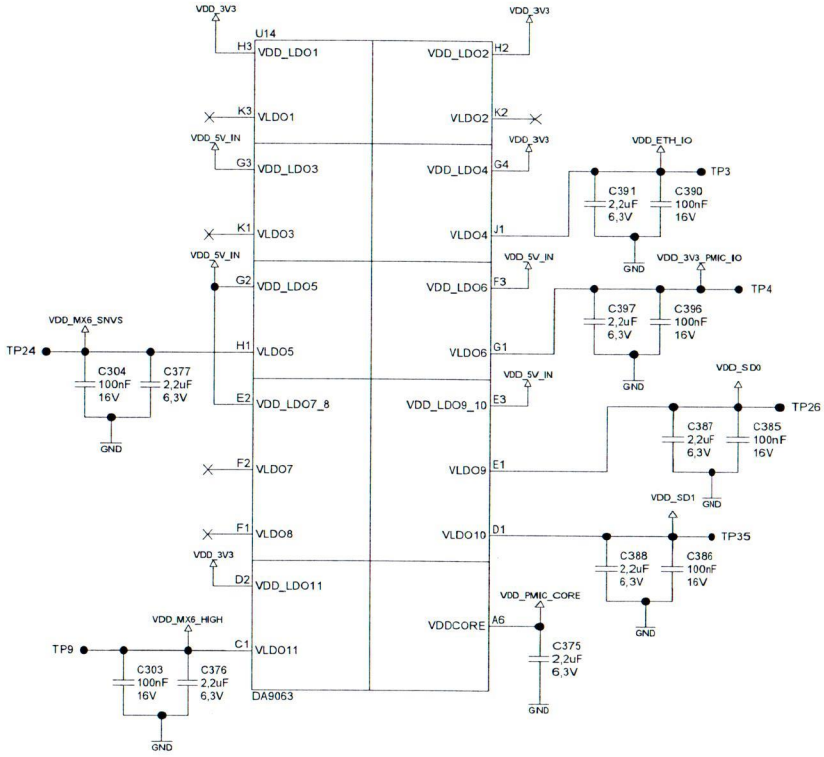
default configuration for other boot sources:

SPI	SPI3, CS0, 3-byte addressing
SD	Normal Boot, SDR12, 4bit, 1 delay cells, SD3, Boot Ack enabled
MMC	Normal Boot, normal speed, 4bit, SD3, Boot Ack enabled
SATA	TX Spread spectr. en., RX spread spec. dis. SATA Gen2 (3,0Gbps), Type i

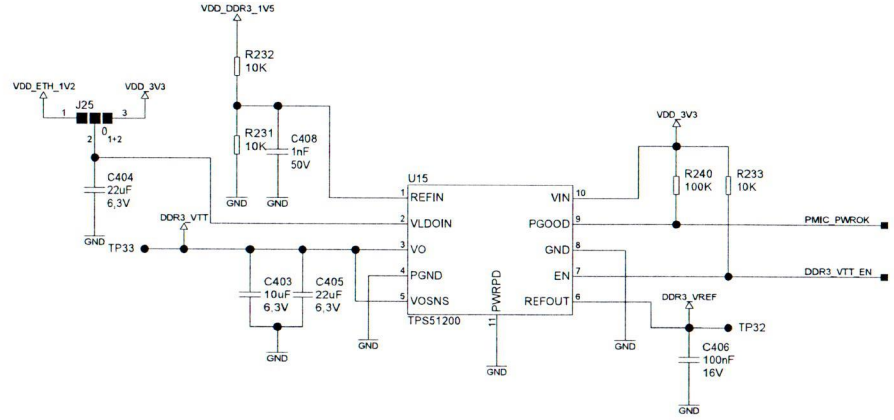
PHYTEC		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6		Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision :002	Sheet 18 of 18

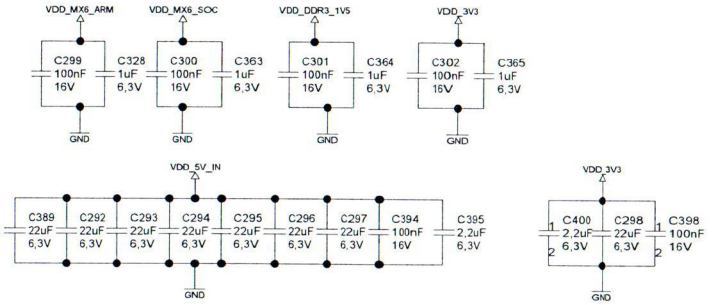
PMIC, Power Supply





DDR3 Reference and Termination





PHYTEC	PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project: PFL-A-02 phyFLEX-i.MX 6	Department: F&E Author: M.Dzierzawa	
01.10.2013	PCB-No.: 1362.2	Revision: 002 Sheet 14 of 18