

PFL-A-02

phyFLEX-i.MX 6

Copyright 2013 PHYTEC TECHNOLOGIE HOLDING AG

INFORMATION IN THIS DOCUMENT IS PROVIDED SOLELY FOR USE IN CONJUNCTION WITH THE PHYTEC PRODUCT DESCRIBED HEREIN. NO INTELLECTUAL PROPERTY RIGHTS -- EXPRESS OR IMPLIED -- ARE GRANTED THROUGH THIS DOCUMENT. LIKEWISE, PHYTEC MAKES NO EXPRESS OR IMPLIED WARRANTIES OF ANY KIND, WHETHER AS TO MANUFACTURABILITY; MERCHANTABILITY; FITNESS FOR A PARTICULAR PURPOSE; OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT. SPECIFICATIONS HEREIN ARE SUBJECT TO CHANGE AT ANY TIME WITHOUT NOTICE.

PHYTEC

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

Department: F&E
Author: M.Dierzawa

Project: PFL-A02-phyFLEX-i.MX 6

01.10.2013 PCB-No.: 13612

Revision 002

Sheet 1 of 18

1

2

3

4

5

6

A

B

C

D

A

B

C

D

1

2

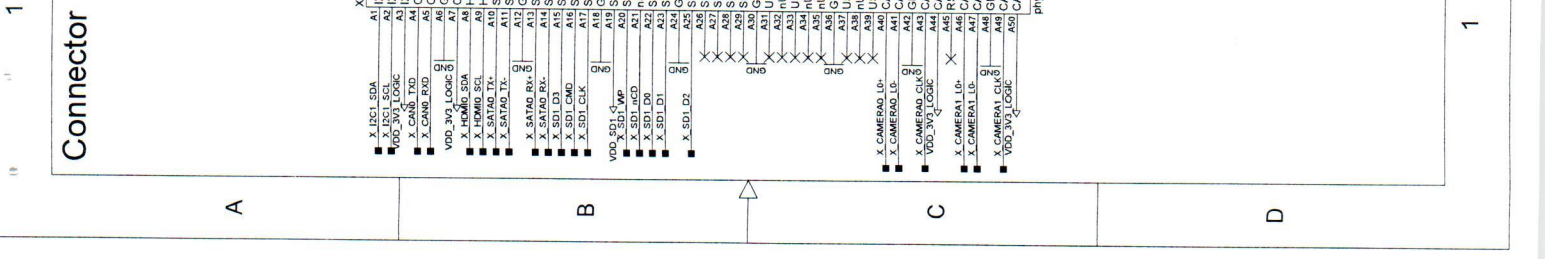
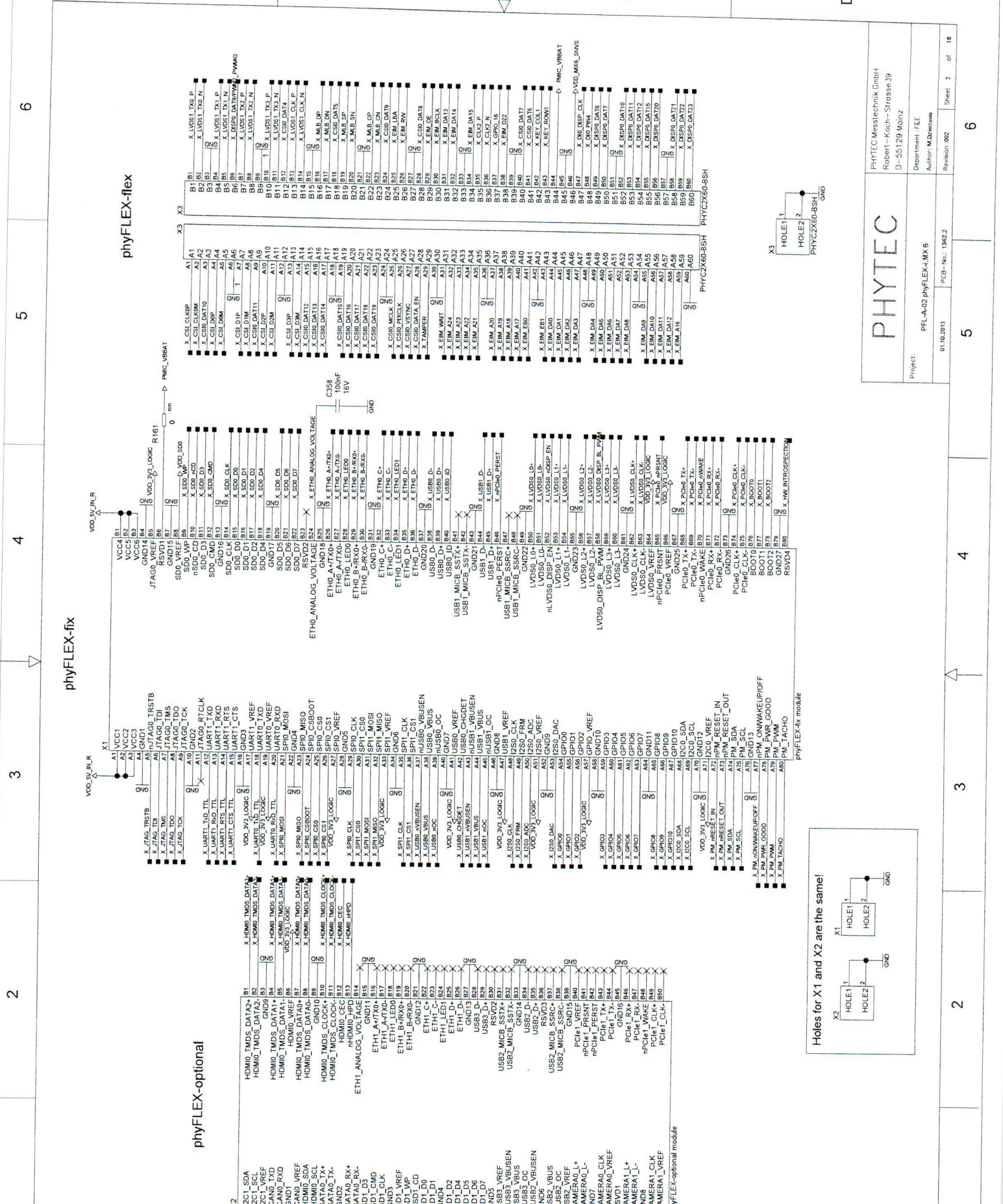
3

4

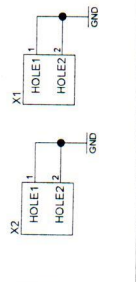
5

6

Connector



Holes for X1 and X2 are the same!



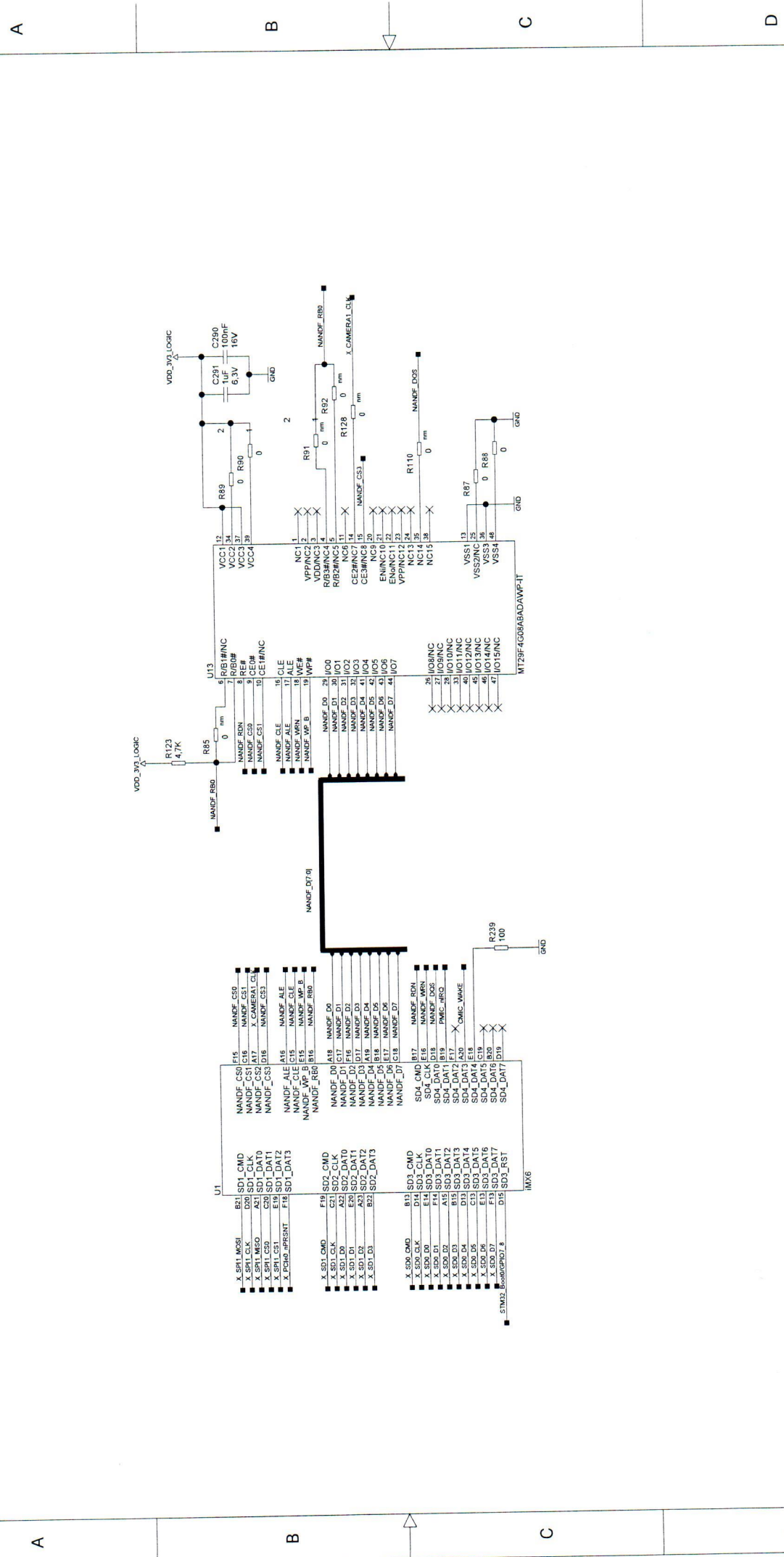
PHYTEC

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

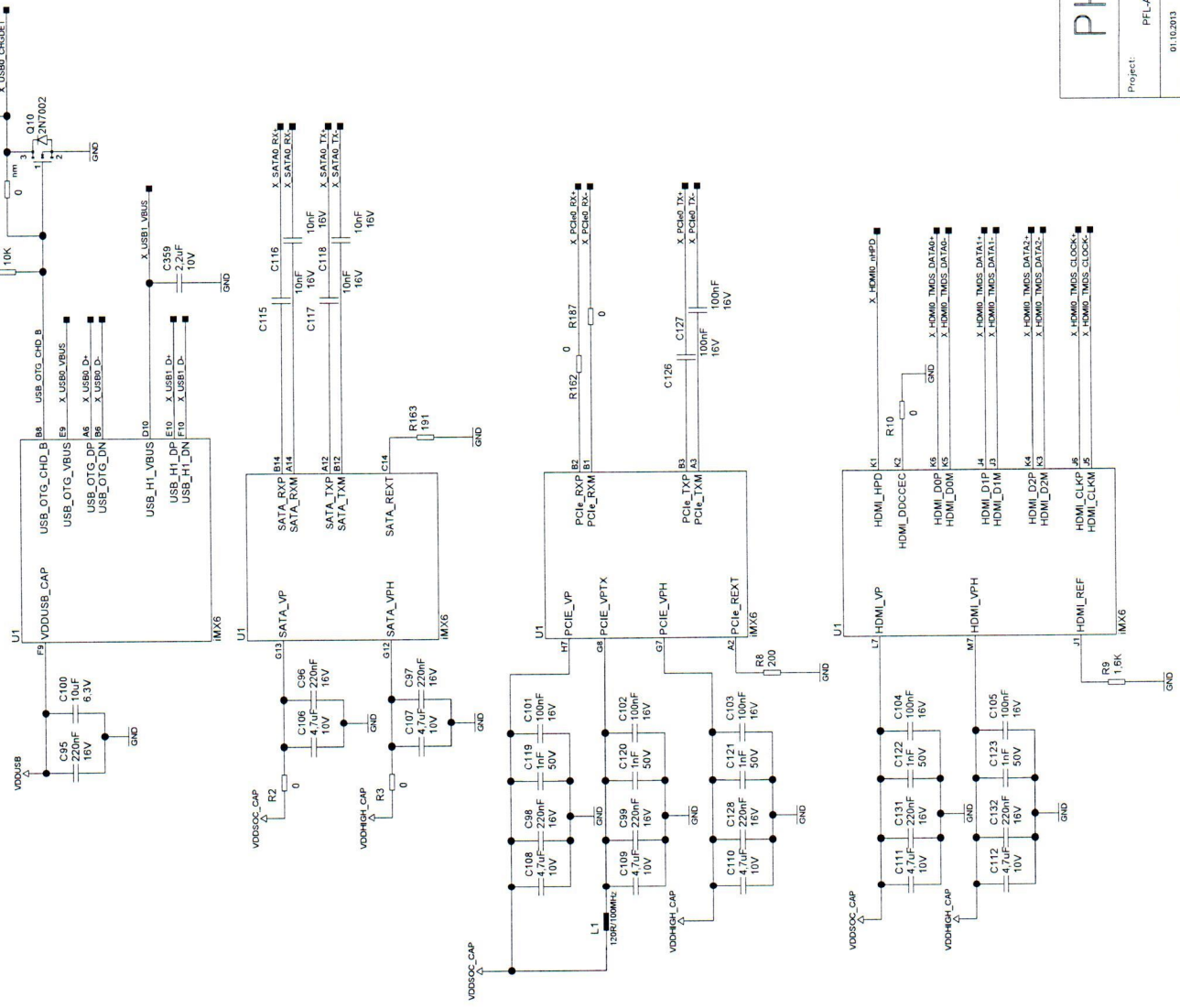
Project: PFL-A02-phyFLEX-I-MX 6
01.10.2013
PCB-Nr.: 1942.2

Department: F&E
Author: M.Dreweira
Revision: 002

SDIO, NAND-Flash



USB Host + OTG, SATA, PCIe, HDMI



<h1>PHYTEC</h1>		Project:	PFLA02 phyFLEX-MX 6	PCB-No.: 13622	Revision: 002	Sheet: 5	of 18
		PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz Department: F&E Author: M.Burawa					

10/100/1000 Ethernet

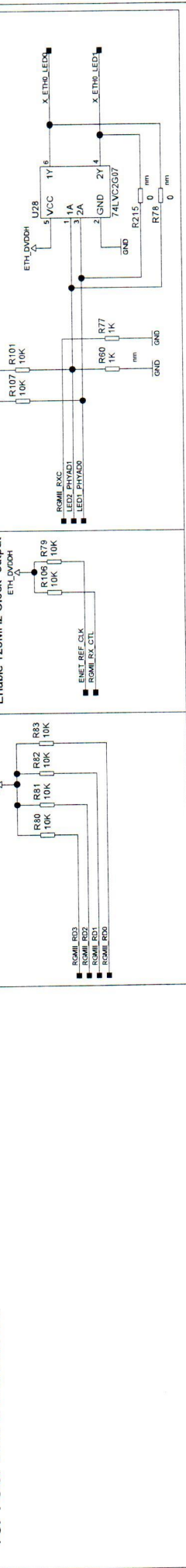
advertise all capabilities

Single LED Mode
Enable 125MHz Clock output

PHY address = 3

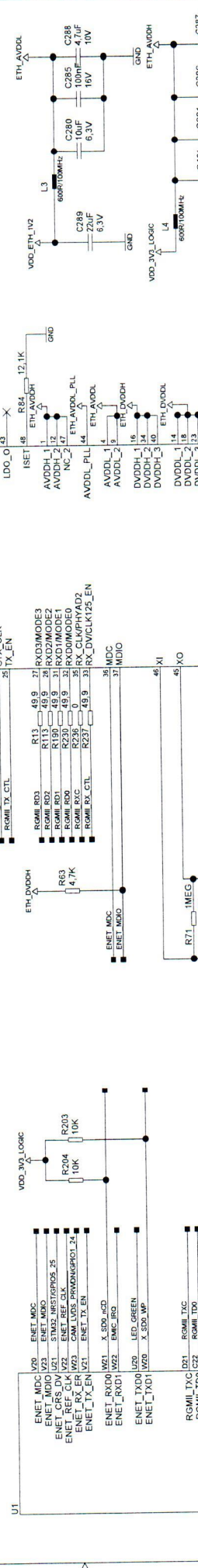
A

A



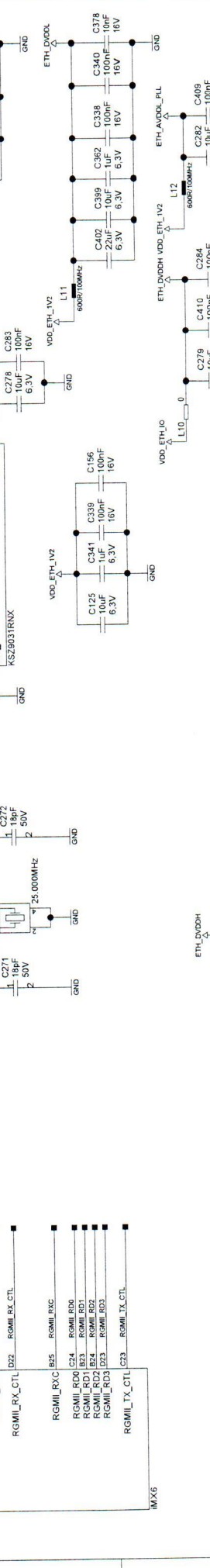
B

B



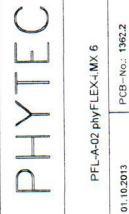
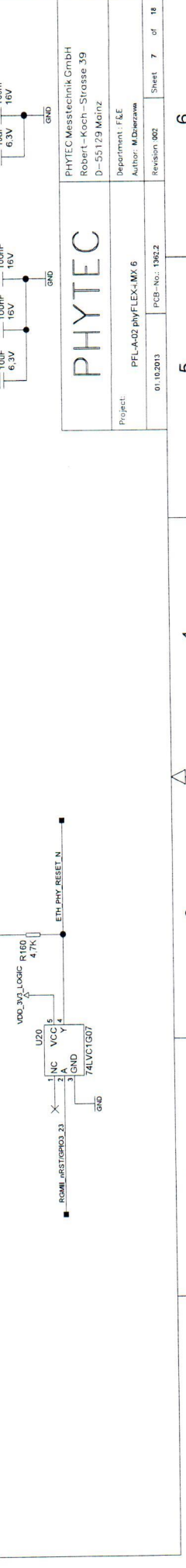
C

C



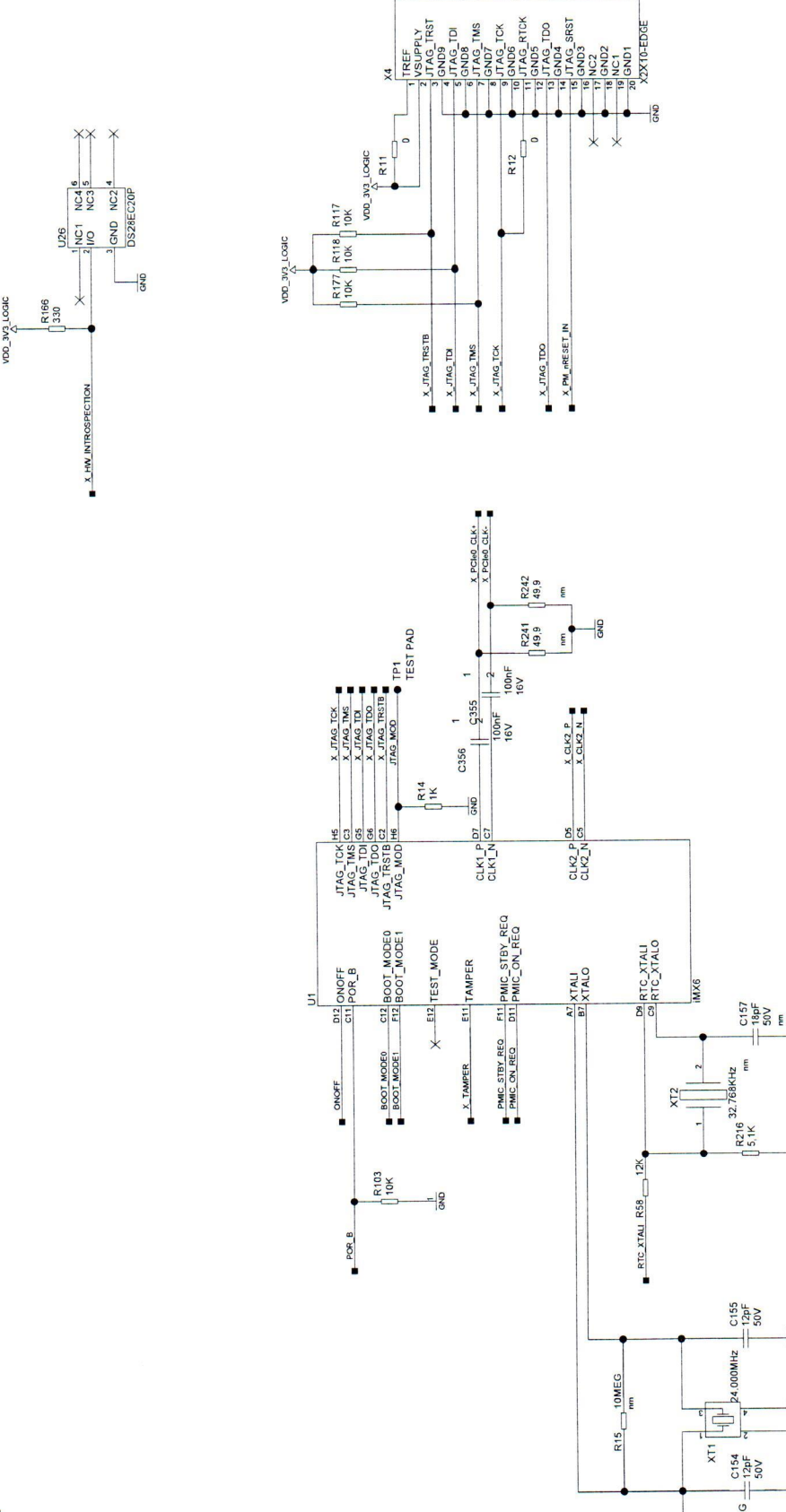
D

D



PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz
Department: F&E
Author: M.Dierzawa

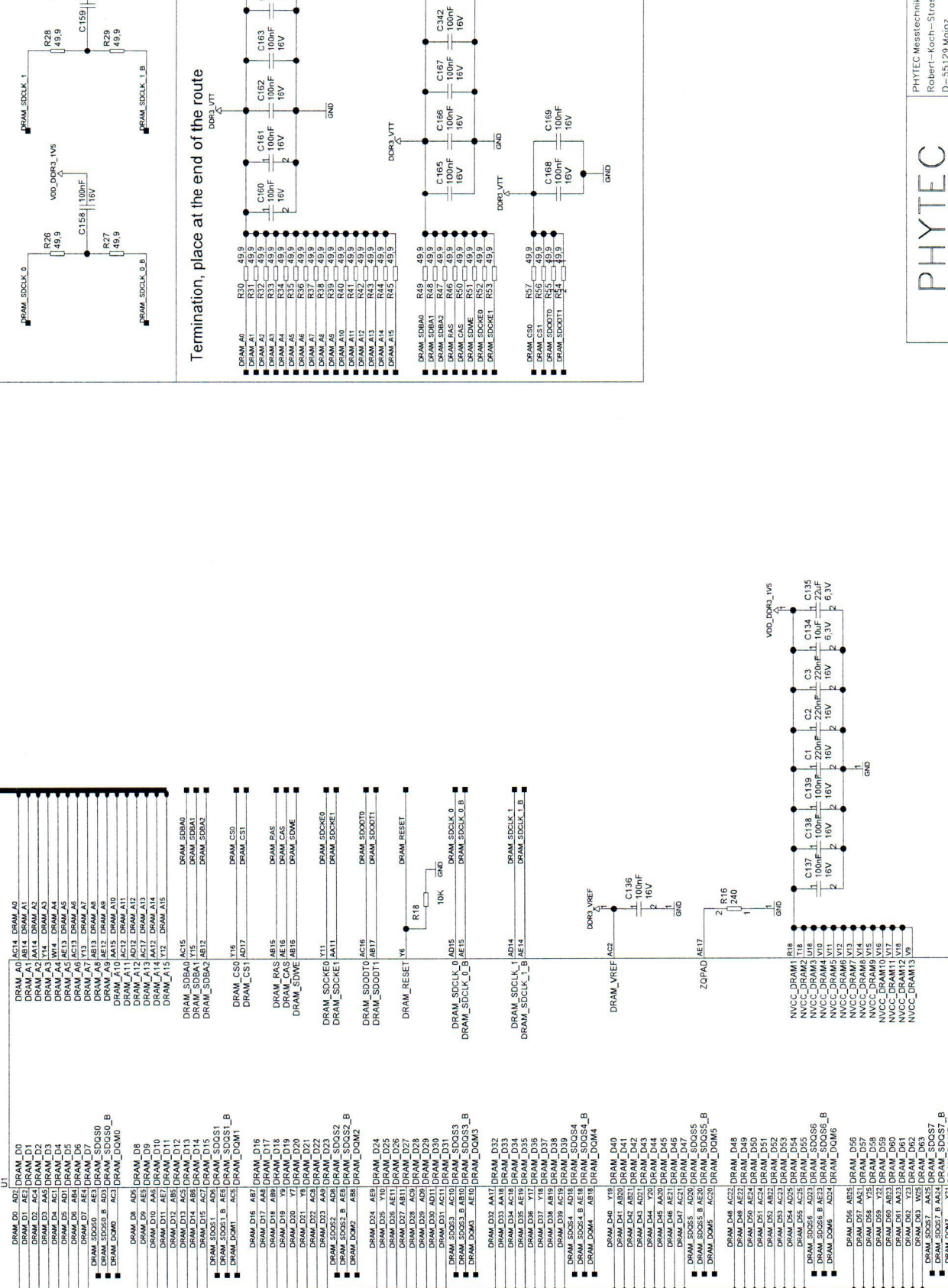
i.MX6 Control



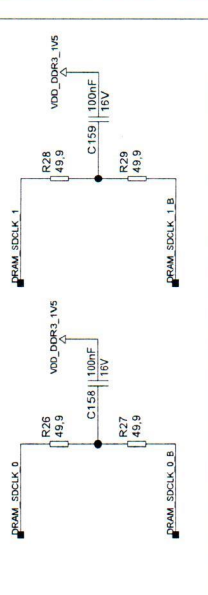
PHYTEC	
Project:	PFL-A02 phyFLEX-i.MX 6
91.10.2013	PCB-No.: 1362.2
Revision 002	Sheet 8 of 18

6 5 4 3 2 1

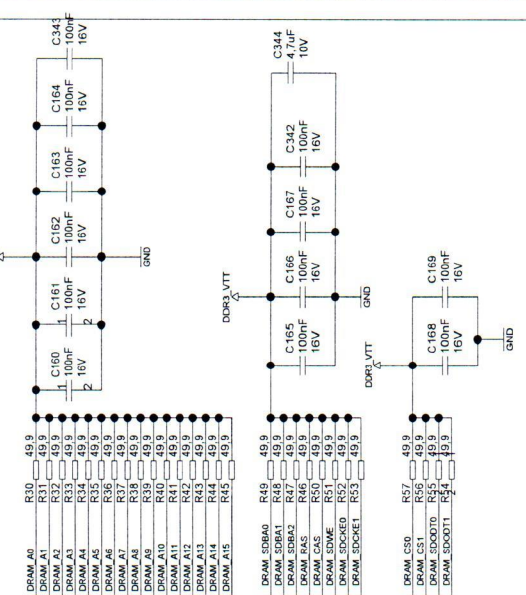
DDR3



Place at the end of the route



Termination, place at the end of the route



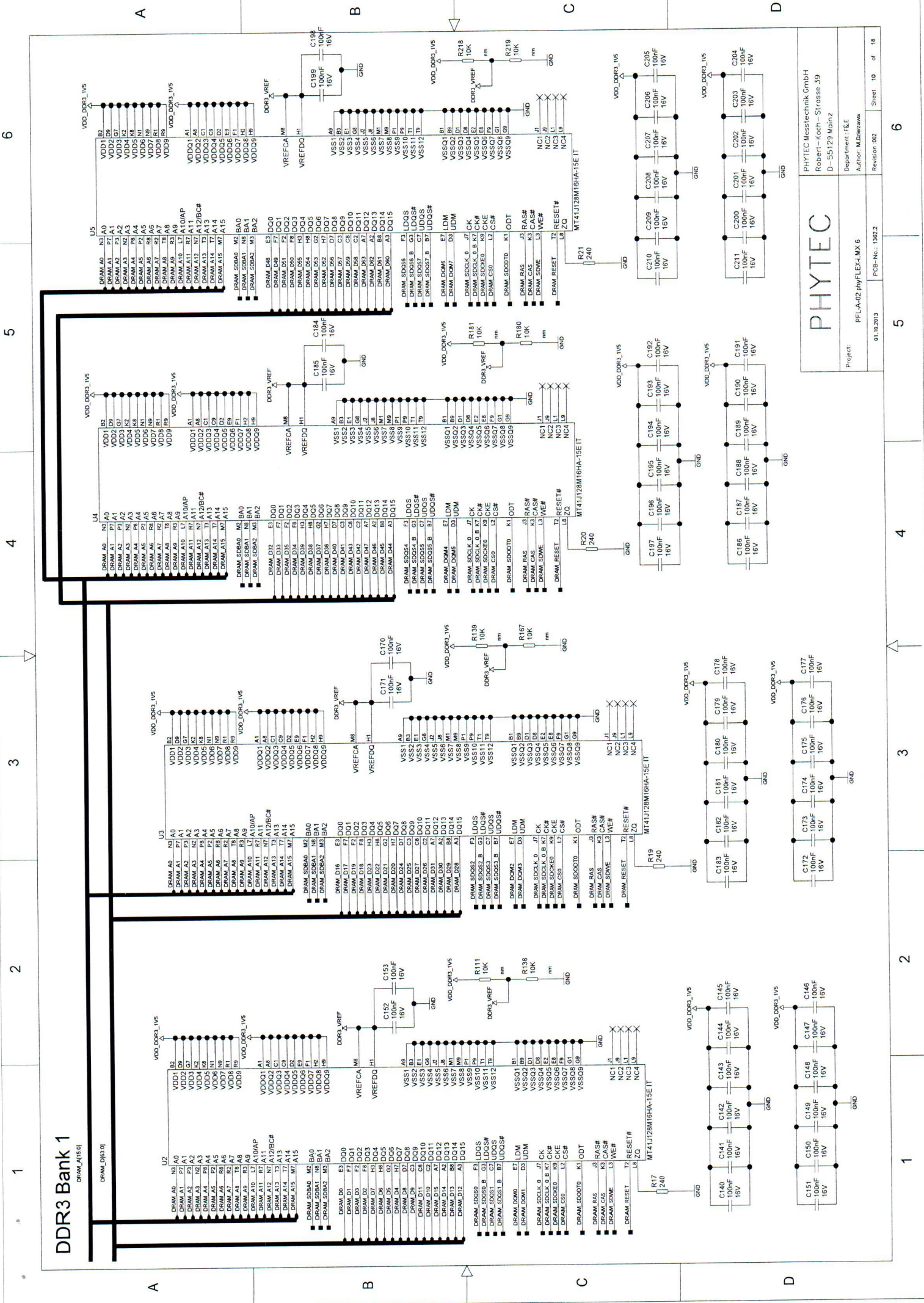
PHYTEC

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

Project: PFL-A-02 phyFLEX-IMX 6
Department: F.EE
Author: M.Dzwawa

01.10.2013 PCE-No.: 1362.2 Revision: 002

6 5 4 3 2 1



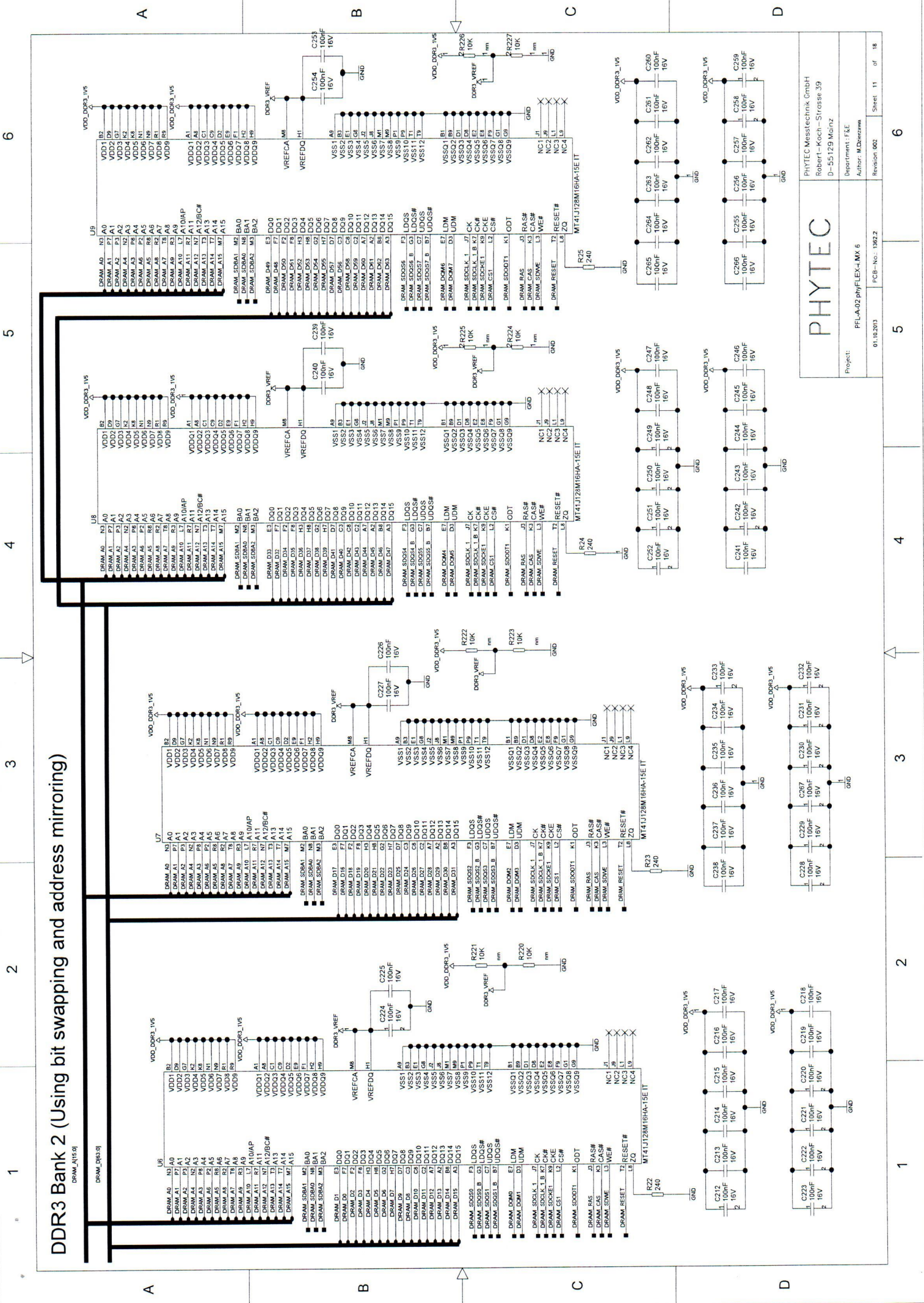
DDR3 Bank 1
DRAM_A1[15:0]

PHYTEC

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

Project: PFLA-02.phyFLEX-1.MX 6
Department: i.F&E
Author: M.Dawatzawa

DDR3 Bank 2 (Using bit swapping and address mirroring)



1

2

3

4

5

6

PHYTEC
 Project: PFL-A02phyFLEX-I-MX 6
 01.10.2013
 FCB-No.: 1062.2

PHYTEC Messtechnik GmbH
 Robert-Koch-Strasse 39
 D-55129 Mainz
 Department: F&E
 Author: M.Dierckow
 Revision: 002
 Sheet 11 of 18

1

2

3

4

5

6

i.MX6 GND



A

B

C

D

A

B

C

D

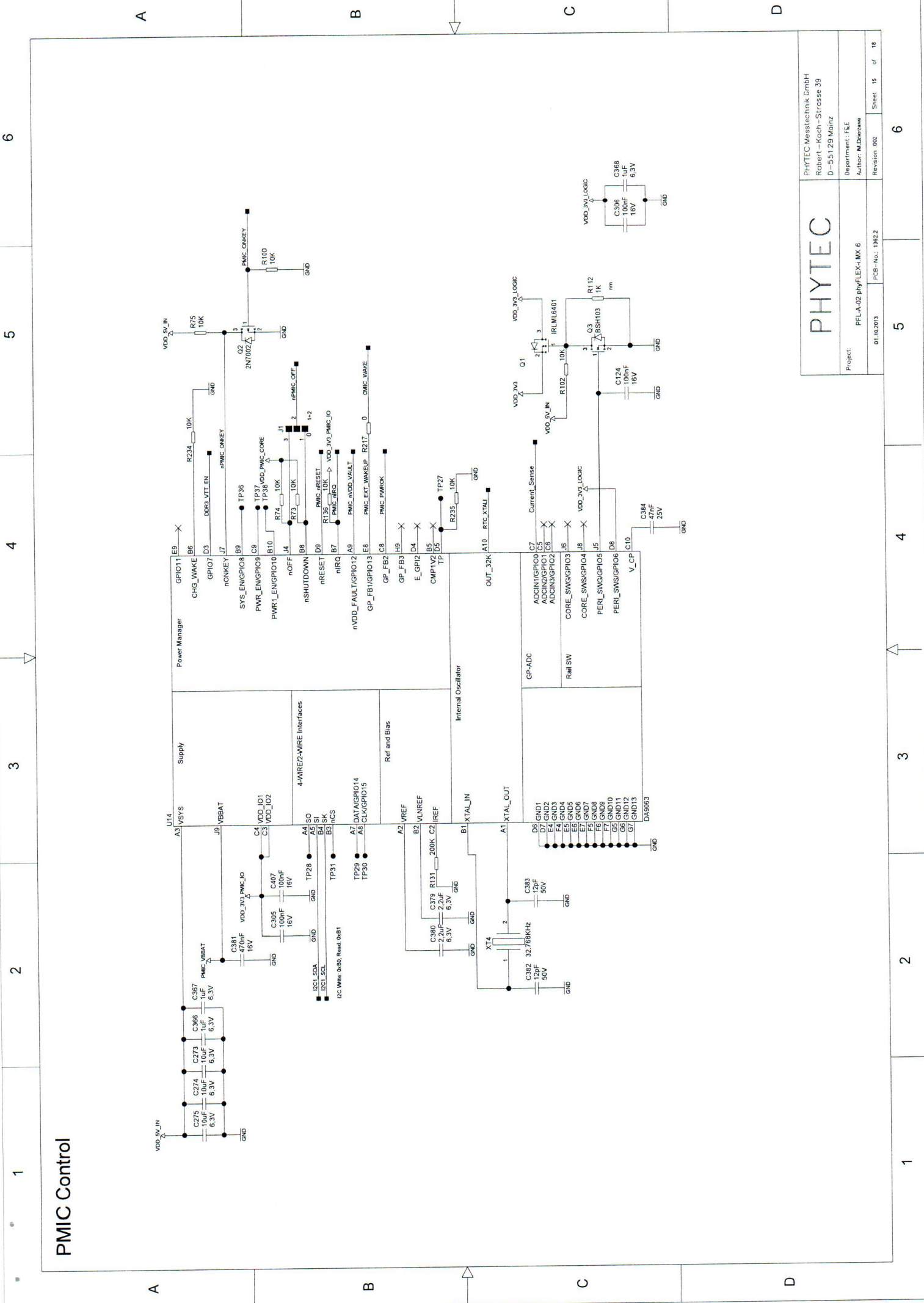
PHYTEC

Project: PFLA-02 phyFLEX-iMX 6
01.10.2013 PCB-No.: 1392.2

PHYTEC Messtechnik GmbH
Robert-Koch-Strasse 39
D-55129 Mainz

Department: F&E
Author: M.Dierzawa

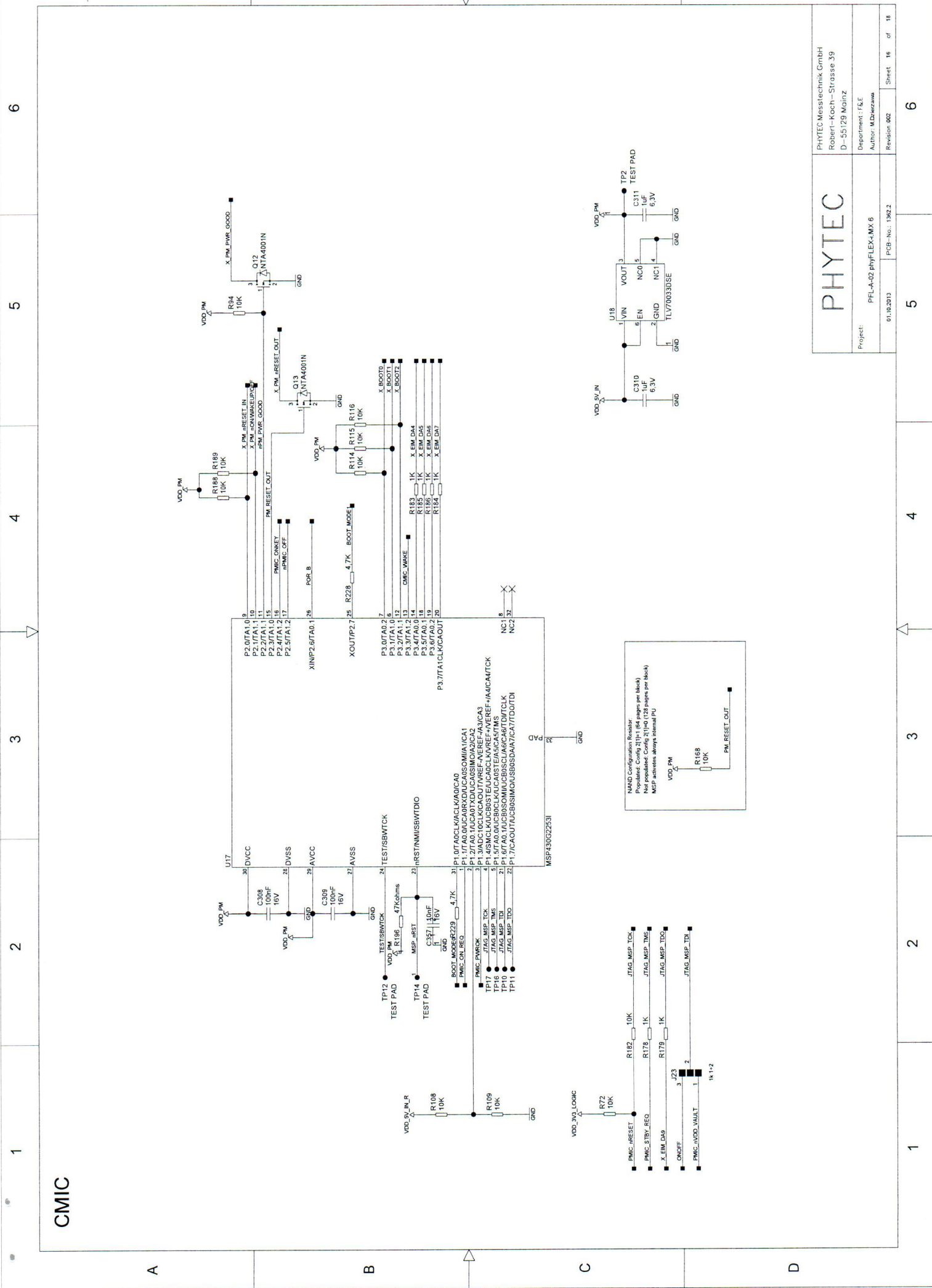
Revision: 002 Sheet: 13 of 18



PMIC Control

PHYTEC	PHYTEC Messtechnik GmbH Robert - Koch - Strasse 39 D-551 29 Mainz
	Department: E&E Author: M.Dierawa
Project: PFLA-02 phyFLEX-4-MX 6	Revision: 002
01.10.2013	PCE-No.: 1362.2
Sheet 15 of 18	

CMIC



PHYTEC

Project: PFL-A-02 phyFLEX-IMX 6
 01.10.2013 PCB-No.: 1392.2 Revision: 002

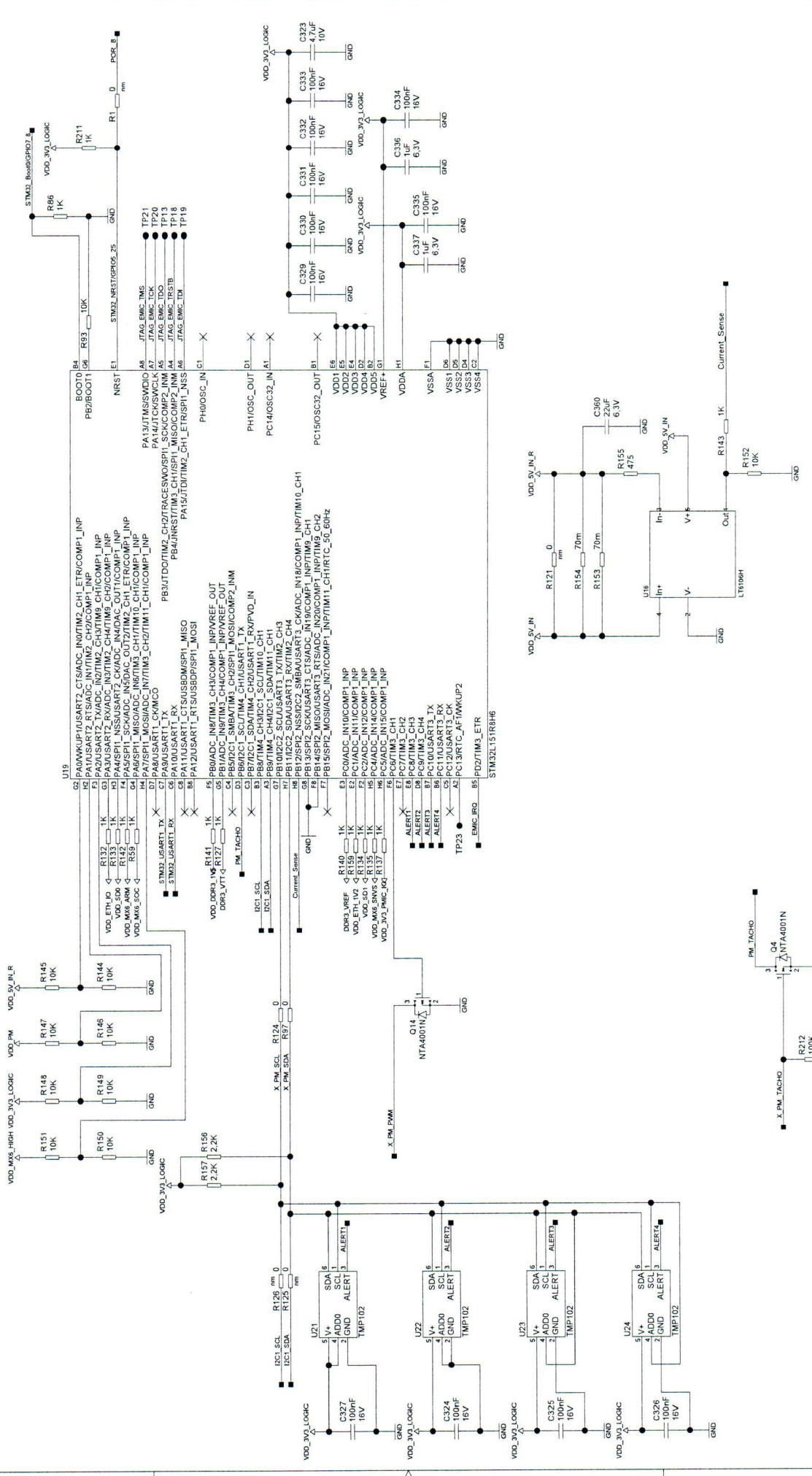
PHYTEC Messtechnik GmbH
 Robert-Koch-Strasse 39
 D-55129 Mainz
 Department: F&E
 Author: M.Dierzawa
 Sheet 16 of 18

PHYTEC

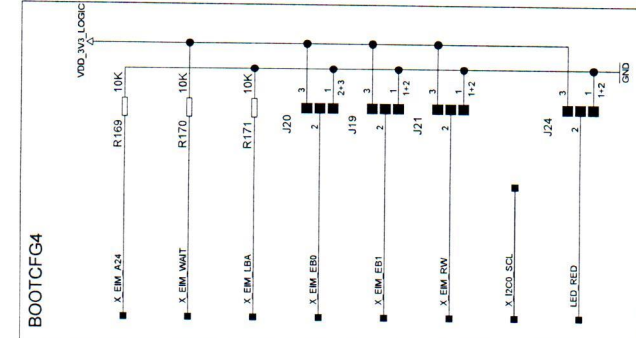
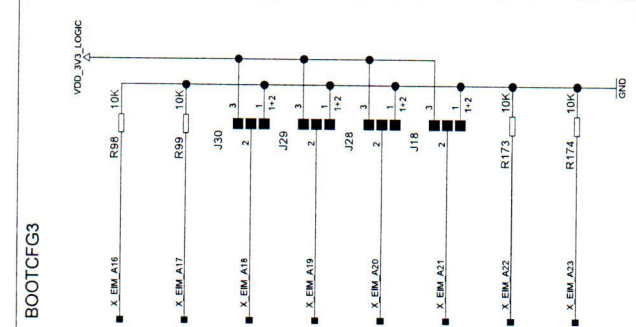
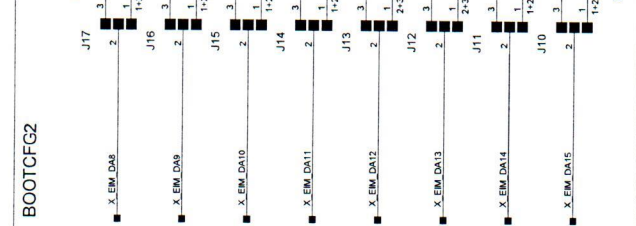
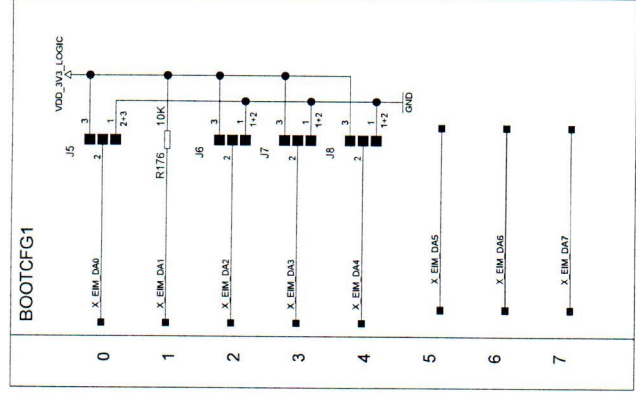
Project: PFL-A-02 phyFLEX-IMX 6
 01.10.2013 PCB-No.: 1392.2 Revision: 002

PHYTEC Messtechnik GmbH
 Robert-Koch-Strasse 39
 D-55129 Mainz
 Department: F&E
 Author: M.Dierzawa
 Sheet 16 of 18

EMIC (optional)



Boot Configuration



Jumpers are 10k

default:

	config[17:0]	config[17:0]	config[17:0]
NAND #80 (64 pages per block)	77790011	00110010	00000000
(7 means that this bit is set by the MSP according to the X_BOOT menu)			

NAND configuration:

	config[17:0]	config[17:0]	config[17:0]
NAND #80 (64 pages per block)	10000011	00110010	00000000
NAND #8208 (128 pages per block)	10000011	00110000	00000000

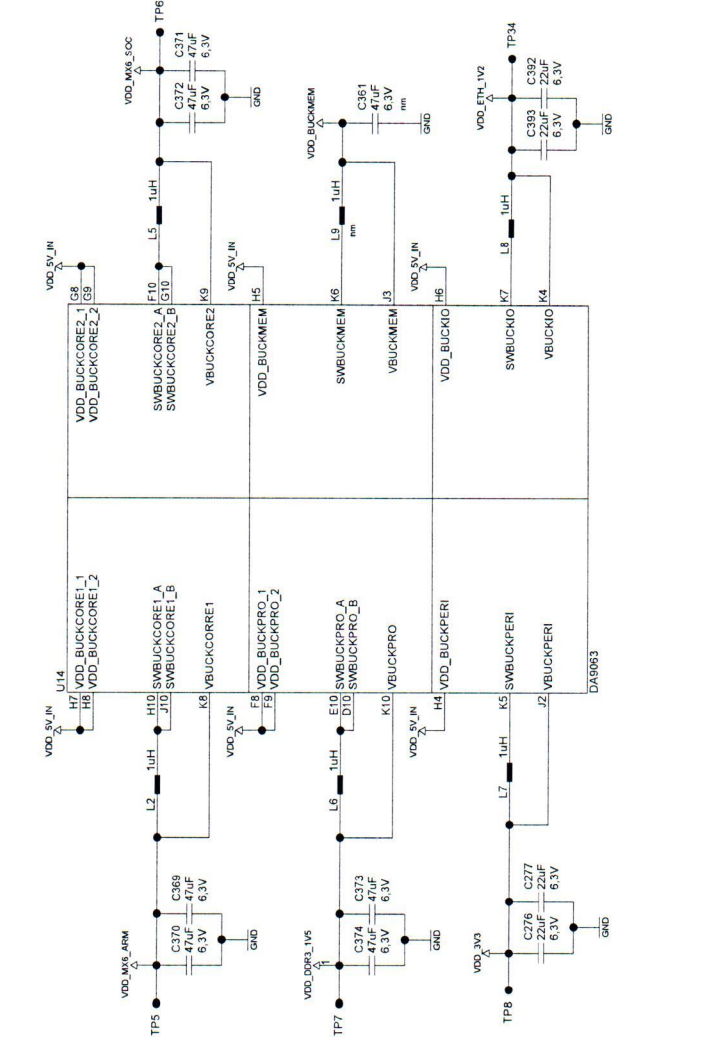
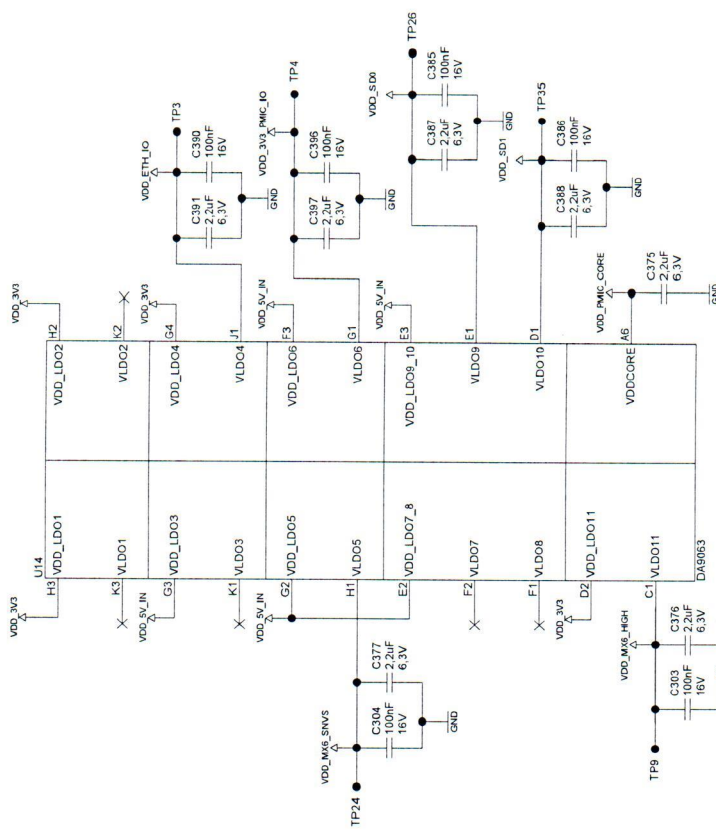
default configuration for other boot sources:

SPI	SPH, CS0, 3-byte addressing
SD	Normal Boot, SDRC (2, 2bit, 1 delay cells, SD3, Boot disk enabled)
MMC	Normal Boot, normal speed, 4bit, SD3, Boot disk enabled
SATA	TX Serial, parallel, RX serial, spec. def, SATA Gen2 (3.0Gbps), Type1

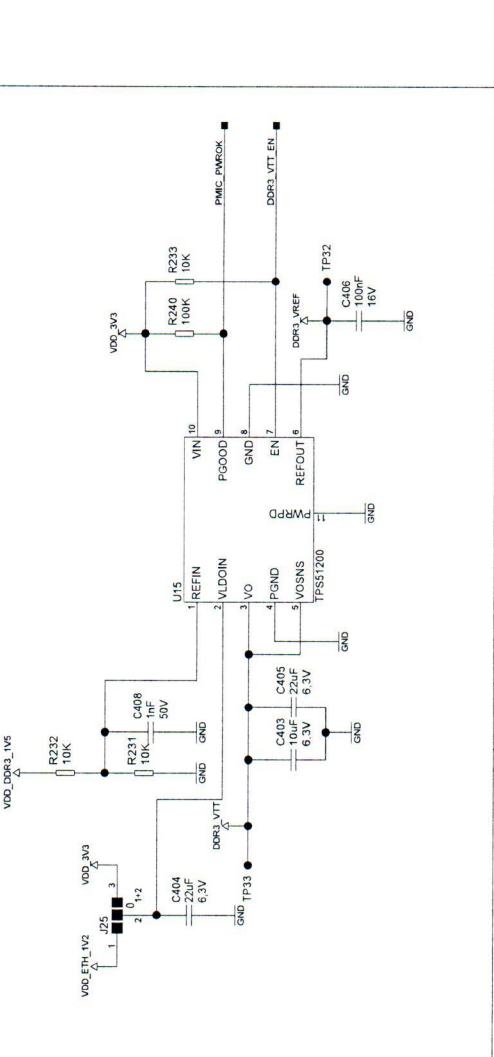
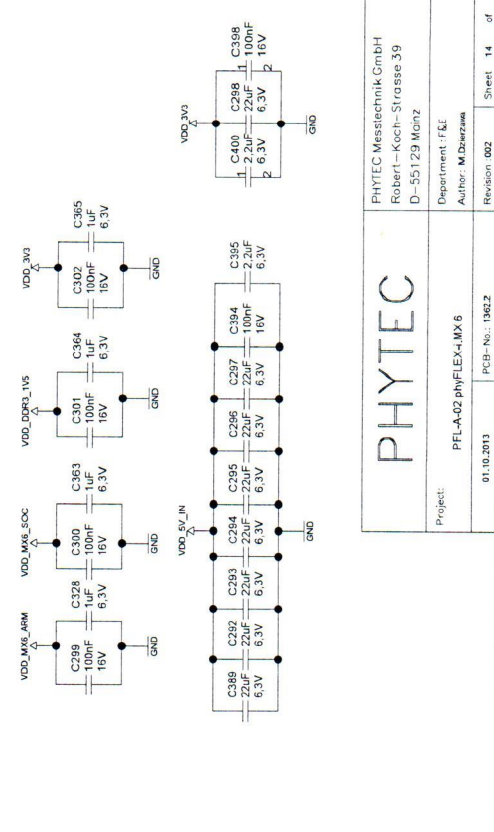
PHYTEC

PHYTEC Messtechnik GmbH Robert-Koch-Strasse 39 D-55129 Mainz	
Project:	PFL-A02 phyFLEX-IMX 6
01.10.2013	PCB-No.: 19622
Revision: 002	Sheet: 18 of 18

PMIC, Power Supply



DDR3 Reference and Termination



PHYTEC

PHYTEC Messtechnik GmbH
 Robert-Koch-Strasse 39
 D-55129 Mainz

Project: PFL-A02-PHYFLEX-1-MX 6
 01.10.2013 PCB-No.: 19652

Department: F&E
 Autor: M.Dawidzka

Revision: 002

Sheet 14 of 18